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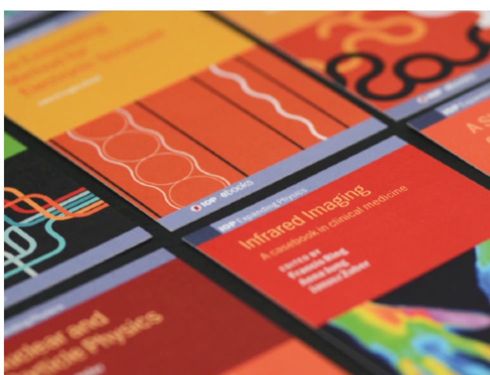

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Monte Carlo simulations of spin transport in nanoscale $In_{0.7}Ga_{0.3}As$ transistors: temperature and size effects

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Abstract

Spin-based metal-oxide-semiconductor field-effect transistors (MOSFETs) with a high-mobility III-V channel are studied using self-consistent quantum corrected ensemble Monte Carlo device simulations of charge and spin transport. The simulations including spin–orbit coupling mechanisms (Dresselhaus and Rashba coupling) examine the electron spin transport in the 25 nm gate length $In_{0.7}Ga_{0.3}As$ MOSFET. The transistor lateral dimensions (the gate length, the source-to-gate, and the gate-to-drain spacers) are increased to investigate the spin-dependent drain current modulation induced by the gate from room temperature of 300 K down to 77 K. This modulation increases with increasing temperature due to increased Rashba coupling. Finally, an increase of up to 20 nm in the gate length, source-to-gate, or the gate-to-drain spacers increases the spin polarization and enhances the spin-dependent drain current modulation at the drain due to polarization-refocusing effects.

Keywords: InGaAs FET, spin transport, Dresselhaus and Rashba coupling, Monte Carlo simulation

(Some figures may appear in colour only in the online journal)

1. Introduction

Transistors using electron spin in their operation have been proposed as an alternative to conventional devices for a number of years to unlock potential novel functionality, reduce power consumption, and increase performance [1, 2]. Among the most promising spin-based semiconductor devices is the spin field-effect transistor (spinFET) [3], a candidate for future high-performance digital computing and memory with ultra low energy needs [4]. The spinFET architecture is similar to that of a conventional semiconductor transistor, with the key difference that the source and drain contacts are ferromagnetic. The source injects spin polarised carriers into the transistor channel. The drain, by contrast, acts as a spin filter by preferentially transmitting carriers, whose magnetic moments align with that of the source [5]. A source-to-drain current can be then modulated by the voltage applied to a gate contact due to a spin rotation caused by the Rashba spin–orbit coupling [6]. This model was generalized to include other effects such as

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spin dephasing due to bulk inversion asymmetry (so called Dresselhaus coupling) [7] and used to predict spin transport effects for 2D III-V heterostructure HEMTs [8, 9].

Spin dephasing is one of the main limiting factors for a spinFET [10, 11]. To minimise the spin dephasing and maximise the spin control [12], a tuning of Rashba coupling was independently suggested [10, 11]. The strength of the Rashba coupling, which depends on the electric field, can be tuned by applying a gate voltage. In theory, we can adjust the gate voltage so that the Rashba coupling effectively cancels the Dresselhaus coupling. However, this approach comes with a significant drawback. The gate bias required to cancel the spin–orbit coupling results in an off-current half of the on-current [13], making such devices unsuitable for digital applications because the off-current must be orders of magnitude smaller (typically 5–8 orders of magnitude) [14]. The simulation data suggests that the on-off ratio would only be around 15%–20% in a real device [15]. Therefore, this work will not consider the transistors based on a tuning of Rashba coupling but will focus on inversion channel FETs [16].

Finally, the FET studied has a $In_{0.7}Ga_{0.3}As$ channel because the control of spin-orbit interaction by a gate voltage was reported experimentally in $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ and $InP/In_{0.77}Ga_{0.23}As/InP$ heterostructures [17, 18]. The FETs with a channel made of InGaAs are intensively studied as potential replacements for Si channels for More Moore digital solutions [19]. The recent advances in the nanoscale InGaAs FETs include gate-all-around nanowire FETs [20, 21], gate-all-around nanosheet FETs [22], and FinFETs [23].

In this work, a new 2D (real space) electron-spin quantum corrected finite-element ensemble Monte Carlo (MC) device simulation tool [24] is employed to investigate the effects of lattice temperature and device dimensions in a 25 nm gate length $In_{0.7}Ga_{0.3}As$ spinFET. The ensemble MC device technique is a semi-classical transport technique for semiconductor devices [25] self-consistently simulating the carrier movement classically and the carrier scattering quantum-mechanically coupled with solutions of Poisson equation (accounting for long-range electron-electron interactions) in a device simulation domain. The 2D MC device simulation tool [26] (i) has incorporated quantum corrections [27, 28] using the effective quantum potential [29], and (ii) has been enhanced to include a non-equilibrium spin transport [24] so is capable to accurately model a highly non-equilibrium electron-spin transport at nanoscale [30].

An electron spinFET brings many advantages into spin based logic operations when compared to the current electron charge based logic. The speed of spin logic operation would be substantially faster, even the increase depends on the efficiency of a spin injection at the source, operational temperature of the spinFET, and on the efficiency of spin detection in the drain. A power dissipation of spin logic operations would be orders of magnitude smaller than a power dissipation of charged electron logic operations. A spinFET would also not suffer from any short channel effects when further scaled down with a tiny off-spin-current, a non-existent DIBL, and a subthreshold slope below 60 mV/dec at 300 K. The overall area of a spinFET would be much smaller than the area of a classical FET allowing for a substantial increase in a spin transistor density on a chip. Finally, a spinFET would be able to operate in a quantum logic, not just in classical logic operations.

This paper is organized as follows. In section 2, the device design and geometry, and the simulation technique are described. In section 3, the underlying theory for the effects of lattice temperature on spin–orbit coupling is summarized, and the simulation results are discussed. In section 4, the effects of device dimensions on spin transport are explored by varying the length of the gate, and the length of the left and right spacers, respectively. Conclusions are drawn in section 5. Finally, two appendices (A and B) collect the parameters used for temperature dependence of band energies, and show a spin polarization angle and a magnitude of the spin polarization along the device channel, respectively.

2. Device design and simulation

2.1. Nanoscale transistor geometry

A nanoscale $In_{0.7}Ga_{0.3}As$ FET, which has been designed as a potential contender to Si metal-oxide-semiconductor FET for the sub-10 nm planar low-power technology [30, 31], is specifically investigated to study the spin transport in a device structure which can be realistically fabricated within the complementary MOS technology [32]. A schematic of the device is given in figure 1. The transistor is fabricated on a Si substrate by growing a 400 nm GaAs buffer layer (using intermediate layers or graded layers or a wafer bonding), a 7 nm thick $In_{0.3}Ga_{0.7}As$ channel grown epitaxially, a 4.6 nm layer of high-κ $Ga_2O_3/(Gd_xGa_{1-x})$(GGO, $\kappa = 20$) separating the channel from a metal gate with a work function of 4.05 eV. The GaAs buffer has a background uniform p-type doping of 1×10^{18} cm^{-3}. The source/drain in the transistor has a n-type Gaussian-like doping including doping extensions, as depicted in figure 1, with a maximum doping of 2×10^{19} cm^{-3}.

A spin transistor requires source and drain contacts that are ferromagnetic, the source acting as a spin injector, the drain contact as a spin detector. Since we are primarily interested in the spin transport along the transistor channel, the spin-injection from the source is assumed to be 100% efficient. The idealistic 100% injection efficiency is often used in spin transport simulations [7, 8, 33, 34] because the injection efficiency depends on particular details of ferromagnetic contact fabrication. The idealistic 100% injection efficiency of the source can be relatively easily adjusted to more realistic injection efficiencies [24]. Highly efficient electrical spin injection has been demonstrated for AlGaAs 2DEGs using Mn doped Esaki diodes with reported efficiencies as high as 75% [35] albeit at extremely low temperatures (less than 4 K).

2.2. Spin transport simulation

The transistor simulations are performed in the device on-region (providing the logical 1 in a binary logic) at a source-drain voltage of 0.7 V and a gate voltage of 0.9 V [30]. The

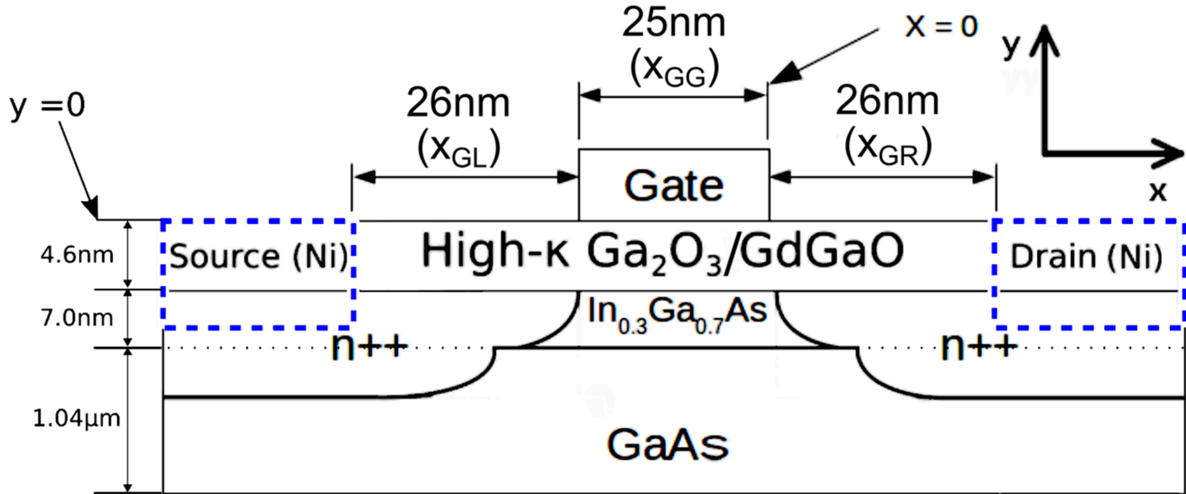


Figure 1. Cross-section of n-channel $In_{0.3}Ga_{0.7}As$ MOSFET with a gate length of 25 nm and indicated lateral and transverse dimensions. The dielectric layer with a thickness of 4.6 nm between the channel and the gate is made of a gallium oxide/gadolinium gallium oxide stack (Ga_2O_3/GdGaO), forming a high-κ dielectric layer with a low density of interface states [27]. The dashed blue lines indicate the position of the source and the drain contacts, which are mimicked by electron reservoirs in the simulations. The labels X_{GL}, X_{GG} and X_{GR} refer to the source-to-gate spacer, the gate length and the gate-to-drain spacer, respectively.

MC simulations are run with 100 000 super-particles in a time step of 1 fs (to minimise plasma oscillations) for a total time of 10 ps. Three injection spin directions are considered with spins aligned parallel to the direction of transport (x axis), the growth direction of the heterostructure (y axis), and the plane of the 2DEG (z axis). The spins of the electrons in the channel are initially assumed to be randomly oriented such that there is no net magnetic field. For each time-step, the average spin polarization vector of the current $\mathbf{S}(t)$ is recorded at the drain contact. The average components of the spin polarization vector are obtained by averaging the individual x, y and z components of the spin polarization vectors of all electrons located at different positions along the channel, in particular at the (left) edge of the drain at the time t. The magnitude of $\mathbf{S}(t) \leqslant 1$ defines the polarization in the direction of $\mathbf{S}(t)$, with 1 corresponding to the maximum spin polarization. This provides a measure of the loss of spin polarisation due to scattering as the electrons traverse the channel.

The angle θ between $\mathbf{S}_{\text{drain}}$ and the injected state $\mathbf{S}_{\text{inj}}$ is given by

$$\theta = \cos^{-1}\left(\frac{|\mathbf{S}_{\text{drain}}|}{\mathbf{S}_{\text{drain}} \cdot \mathbf{S}_{\text{inj}}}\right).$$

The magnitude and the angle of the polarization vector determine the expected modulation of the drain current, $\xi(M_D, \theta)$ (equation (9) [24]) as

$$\xi(M_D, \theta) = \frac{1 + M_D \cos\theta}{1 + M_D} \tag{1}$$

where $M_D = |\mathbf{S}_{\text{drain}}|$ is the magnitude of the polarization vector at the drain edge. For $\theta = 0$, we have $\xi(M_D, \theta) = 1$. This motivates the definition of the spin-dependent drain current modulation, V_S, as

$$V_S(M_D, \theta) = 1 - \xi(M_D, \theta) = \frac{M_D}{M_D + 1}(1 - \cos\theta) \tag{2}$$

in the following referred to simply as the spin modulation. V_S ranges from 0 for $\theta = 0$ to 1 for $\theta = 180°$ and $M_D = 1$ and is a measure distinguishing the on- and off-state from the drain current. Maximum modulation requires a high spin polarization and a large effective rotation angle θ.

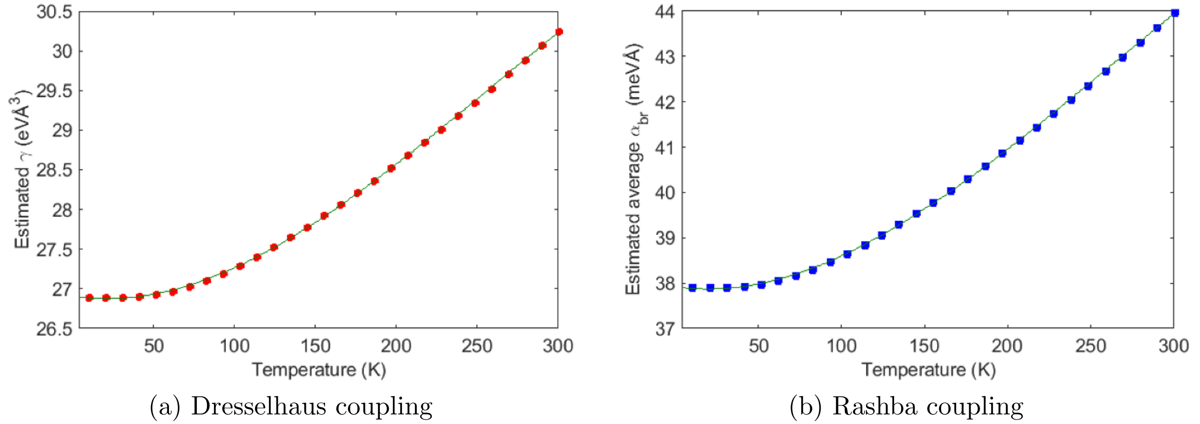
In the following, when we refer to the (spin) polarization angle, we shall imply the angle θ of the polarization vector at a given time or point in space relative to the initial polarization vector of the injected spins, while (spin) polarization shall refer to the magnitude of the (spin) polarization vector. Spin polarization always refers to the electron spins, and we shall often simply use polarization.

3. Temperature dependence

Our first aim is to explore the temperature dependence of the spin polarization at the drain edge for a fixed geometry and at a fixed gate voltage. The former depends primarily on the temperature dependence of the Rashba and Dresselhaus coupling. All characteristics of the spin transistor (spin polarization, spin angle) are monitored by averaging physical quantities of interest over the all particles and a simulation time as usual in the MC technique [25], with the temperature dependence taken into account through the change in energy assuming a Fermi–Dirac distribution [30].

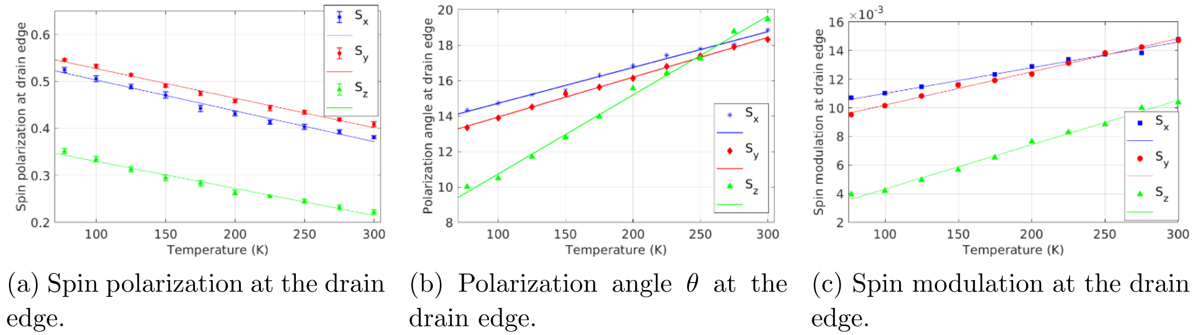
3.1. Rashba and dresselhaus coupling

The temperature dependence of Dresselhaus and Rashba parameters γ and α_{br} relates to the temperature dependence of the lattice constant a_0, leading to an increase in the band energies



(a) Dresselhaus coupling (b) Rashba coupling

Figure 2. Temperature dependence of Dresselhaus (γ) and Rashba (α_{br}) coefficients in $In_{0.7}Ga_{0.3}As$ between 4 and 300 K. The Rashba coefficient is estimated using an average electric field of 4.219 $\times 10^7$ V m^{-1} present at $V_G = 0.7$ V and $V_D = 0.5$ V. The dark green lines are cubic fits to the data. The shape of the Rashba curve agrees well with similar calculations for GaAs [36].



(a) Spin polarization at the drain edge. (b) Polarization angle θ at the drain edge. (c) Spin modulation at the drain edge.

Figure 3. Lattice temperature dependence of the spin polarisation, the spin polarisation angle θ, and the spin modulation, all at the drain edge at $V_G = 0.9$ V and $V_D = 0.7$ V. The linear fits elucidate trends.

E_0, E_1, Δ_0 and Δ_1 with decreasing temperature. This effect has been studied for GaAs [37, 38], and the temperature dependence of the bandgap energies for GaAs has been investigated experimentally [38, 39], leading to the relation

$$E_g(T_L) = E_{g0} - \alpha_B \left(1 + \frac{2}{\exp(\theta/T_L) - 1}\right), \tag{3}$$

where T_L is the lattice temperature and the parameters E_{g0}, α_B and θ are obtained by fitting experimental data. The temperature dependence for InAs, needed to fit a $In_xGa_{1-x}As$ ternary compound, with x being the content of In, is not as well documented in the literature, with only limited experimental data for the fitting parameters θ and α_B published for the interband energies [40, 41]. The fitting parameters used to calculate the band energy dependence in our simulations are listed in table A1 in appendix A. The resulting dependence of the Dresselhaus (γ) and Rashba (α_{br}) coefficients as a function of the lattice temperature is shown in figure 2. Both coefficients increase non-linearly due to the changes in the interband energies, both varying cubically as expected. The shape of the Rashba curve fits well with similar calculations for GaAs [36].

3.2. Polarization at drain edge

The spin dynamics are explored between 77 and 300 K at a gate voltage (V_G) of 0.9 V and a drain voltage (V_D) of 0.7 V (the transistor drive bias [32]). Note that the $In_{0.7}Ga_{0.3}As$ FET has a threshold voltage (V_T) of 0.2 V as required to provide $V_G - V_T \equiv V_D = 0.7$ V [26, 27]. This covers practical temperatures from liquid nitrogen cooling up to room temperature, in which the MC simulator using the Fermi–Dirac statistics has been tested [42]. Figure 3(a) shows that the spin polarization across the device channel increases linearly with decreasing temperature. The lowering of the temperature decreases the number of electron scattering events as the electrons travel through the channel, which is expected to decrease the decay of the spin polarization, therefore leading to a higher net spin polarization at the drain edge. However, both the Rashba and Dresselhaus coupling also decrease with temperature, which reduces the rotation angle θ between the initial spin polarization and the spin polarization at the drain edge, as shown in figure 3(b). Indeed, for S_z injection polarization, the rotation angle θ at 300 K is about twice as large as for 77 K. Thus, we have two competing effects, increasing spin polarization and decreasing rotation angles. Combining both effects shows that the latter is dominant, i.e., the spin modulation by the gate

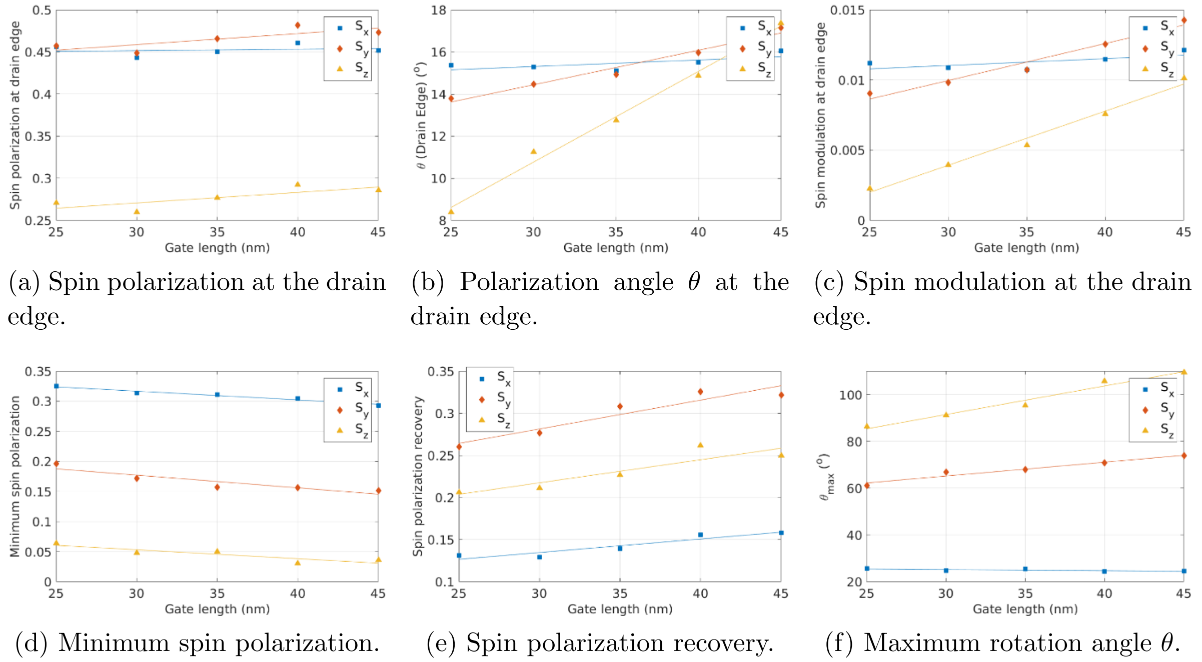


Figure 4. Spin polarization, rotation angle θ, spin modulation (equation (2)), all at the drain, then minimum spin polarization, spin polarization recovery, and maximum rotation angle θ_{max} in x, y, and z directions (symbols) as a function of the gate length ($V_G = 0.9$ V and $V_D = 0.7$ V) with linear fits (full lines) to elucidate trends.

actually *increases* with increasing temperature (figure 3(c)) due to increasing spin-orbital Dresselhaus and Rashba coupling of electrons with increasing temperature. This spin-orbital coupling is induced by the high electric fringing field present beneath the gate, especially, at the drain side of the gate [43].

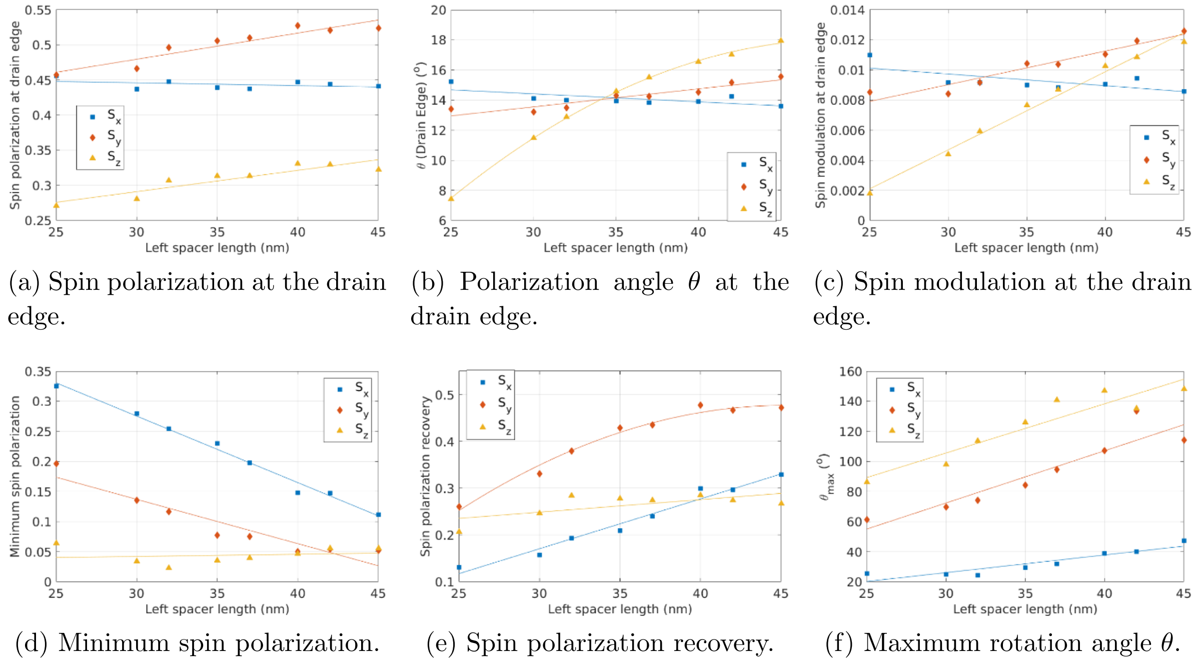
4. Device scaling

In this section, we aim to elucidate the effect of the device scaling on the drain edge polarization. Therefore, a spin polarization, a rotation angle θ, and a spin modulation defined by equation (2) at the drain contact are plotted in figures 4 and 5 together with a minimum spin polarization, a spin polarization recovery, and a maximum rotation angle θ_{max} in x, y, and z directions at operational bias of a gate voltage of 0.9 V and a drain voltage of 0.7 V (a so-called drive voltage). The spin polarization at the drain edge is an average spin polarization of all electrons entering the drain (modelled by a reservoir in the simulations) over all simulation time. All the following quantities are obtained also by averaging all electrons along the channel over all simulation time. The rotation angle of the polarization at the drain edge is a cumulative effect of the Rashba and Dresselhaus coupling experienced by electron spins as they move across the channel. The minimum spin polarization is the lowest spin polarization occurring along the channel, the spin polarization recovery is the difference between the spin polarization at the drain edge and the minimum of the spin polarization along the channel, and the maximum rotation angle θ_{max} is the maximum polarization angle reached along the channel.

If the channel length, or the distance between the gate and the source, or the distance between the gate and the drain (so-called spacers) is decreased/increased, the spatially distributed electric field will increase/decrease, affecting the spin-orbital coupling. Therefore, we vary the three transistor design parameters: the length of the gate (X_{GG}) shown in figure B1, the distance between the gate and the source (X_{GR}) in figure 5, and the distance between the gate and the drain (X_{GL}) in figure 6. All other device dimensions and material parameters (e.g., the thickness of the layers in the y-direction and their composition) remains the same.

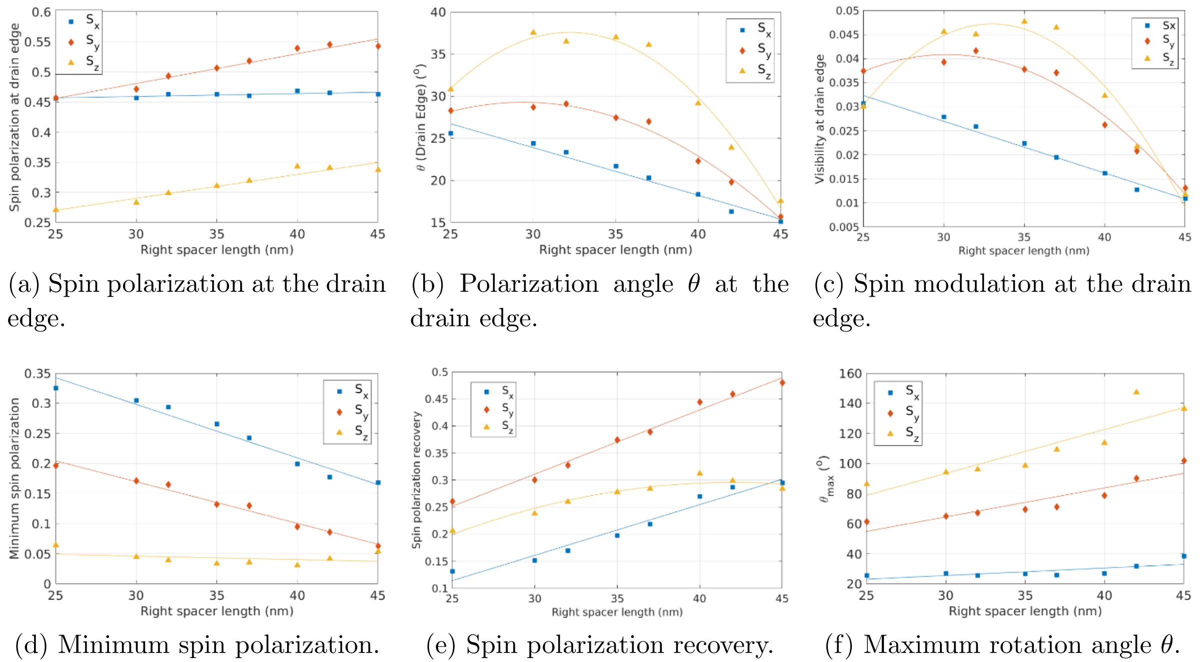
4.1. Gate length dependence

The gate length is varied from 25 to 45 nm (see figure 1) while the spacer distances are fixed, i.e., 25 nm for X_{GG} and 26 nm for X_{GL} and X_{GR}. Since increasing the gate length increases the length of the channel, the spin polarization at the drain edge should decrease with the increasing gate length. However, figure 4(a) does not show any decrease in the spin polarization at the drain edge with increased gate length. For S_y and S_z initialized spins, the spin polarization at the drain edge slightly increases. This behaviour is clearly evident in the spin polarization along the channel plots in figures B1(d)–(f) and is consistent with earlier simulation results [24] indicating that the spin polarization does not decrease monotonically along the channel, as it might be expected if the spin polarization decayed exponentially. Rather, analysis of the spin



(a) Spin polarization at the drain edge.
(b) Polarization angle θ at the drain edge.
(c) Spin modulation at the drain edge.
(d) Minimum spin polarization.
(e) Spin polarization recovery.
(f) Maximum rotation angle θ.

Figure 5. Spin polarization, rotation angle θ, spin modulation (equation (2)), all at the drain, then minimum spin polarization, spin polarization recovery, and maximum rotation angle θ_{max} in x, y, and z directions (symbols) as a function of the source-to-gate spacer length ($V_G = 0.9$ V and $V_D = 0.7$ V) with fits to elucidate.



(a) Spin polarization at the drain edge.
(b) Polarization angle θ at the drain edge.
(c) Spin modulation at the drain edge.
(d) Minimum spin polarization.
(e) Spin polarization recovery.
(f) Maximum rotation angle θ.

Figure 6. Spin polarization, rotation angle θ, spin modulation (equation (2)), all at the drain, then minimum spin polarization, spin polarization recovery, and maximum rotation angle θ_{max} in x, y, and z directions (symbols) as a function of the gate-to-drain spacer length ($V_G = 0.9$ V and $V_D = 0.7$ V) with linear fits to elucidate trends.

polarization as a function of the position along the channel suggests that the initial decay is small, resulting in a marginally reduced minimum spin polarization (figure 4(d)), but this decrease is more than offset by an increased spin polarization recovery (figure 4(e)). The recovery of the spin polarization (akin to a refocusing effect in an NMR system [44]) in the gate-to-drain spacer region, where a large fringing field occurs, was reported previously [24].

At the same time, since the spin–orbit coupling mediated by a large fringing electric field [45] surrounding the region

beneath the gate acts over a longer distance, one might expect the polarization angle of the polarization to increase with the increasing gate length, and indeed, both figures B1(a)–(c) and 4(f) show an increase in the maximum polarization angle achieved. Although this increase is followed by a steeper drop between the gate and drain with increasing gate length, figure 4(b) still shows a linear increase of the polarization angle of the polarization at the left drain edge if the spins are initially S_y and S_z polarized. Combined, the increase in both the spin polarization and the polarization angle at the drain edge with increasing gate length results in an overall spin modulation increase with the gate length for S_y and S_z polarization, as shown in figure 4(c). For S_x polarization, the effect of increasing the gate length on the spin polarization, polarization angle and spin modulation at the drain edge appears to be neutral.

4.2. Source-to-gate/gate-to-drain spacer

The effect, if any, of increasing the source-to-gate spacer length is less obvious to analyse. A simple model would suggest that increasing the source-to-gate spacer length would be detrimental to the spin polarization at the drain edge due to the increased channel length, and we previously conjectured that increasing the source-to-gate spacer length does not increase the Rashba and Dresselhaus coupling, which leads to the rotation effect and increase in the polarization angle (relative to the initial polarization vector). However, figure 5(f) suggests the maximum polarization angle does in fact increase with increasing source-to-gate spacer lengths. Furthermore, figure 5(a) suggests that increasing the source-to-gate spacer length increases the spin polarization at the drain edge, at least for S_y and S_z polarization, while the effect is neutral for S_x polarization. A similar effect is observed for the polarization angle θ. Figure 5(f) shows that the maximum polarization angle increases in all cases, but the increase is partly offset by a steeper decrease between the gate and drain (figures B2(a)–(c)). As a result (figure 5(b)) we observe a small net increase in the polarization angle at the drain edge for S_y and S_z, while the effect is neutral for S_x polarization. Combining the effect of increasing the source-to-gate spacer length on the spin polarization and polarization angle leads to an increase in the spin modulation at the drain edge for S_y and S_z polarization, but a neutral or marginally detrimental effect for S_x polarization (figure 5(c)). We also observe a decrease in the minimum spin polarization along the channel (figure 5(d)), which is consistent with our expectations that increasing the distance between the source and gate contacts (X_{GL}) decreases spin polarization as the electrons spend more time in the source-to-drain region of the channel, thus experiencing more scattering events, before being influenced by the fringing field generated by the gate. However, the source-to-gate polarization is partially offset by a stronger spin polarization recovery in the gate-to-drain region of the channel (see figures 5(e) and B2(d)–(f)).

When it comes to increasing the gate-to-drain spacer length, the results are more interesting. Except for S_z polarization, where the effect is neutral, the minimum spin polarization along the channel decreases (figure 6(d)). However, the decrease is compensated for by an increase in the spin polarization recovery (figure 6(e)), because the spin polarization has more time to refocus, resulting in a slight increase in the spin polarization at the drain edge for S_y and S_z polarization, and a neutral effect for S_x (figure 6(a)). In all cases, we observe that the spin polarization increases or remains constant with increasing the gate-to-drain spacer length. Again, this is consistent with the refocusing hypothesis and conflicts with a simple model that predict a monotonic decrease in the spin polarization with the channel length [46]. In addition to the increase in the overall spin polarization, figure 6(f) also shows an increase in the maximum polarization angle θ_{max} with increasing right spacer length. However, this increase is more than offset by a sharper drop in the polarization angle between the gate and drain, resulting in a decrease of the polarization angle θ at the drain edge with the distance between the gate and drain (figures 6(b) and B3(a)–(c)). For S_y and S_z polarization, the dependence of θ_{max} and θ at the left drain edge on the gate-to-drain length appears to be non-linear, resulting in a similar non-linear dependence of the spin modulation (figure 6(c)). In particular, the latter graph suggests that there may be an optimum gate-to-drain spacer length that maximizes the spin modulation for S_y and S_z, while increasing the gate-to-drain spacer length appears to be overall detrimental to the spin modulation for S_x polarization.

5. Conclusions

Spin transport in a nanoscale $In_{0.7}Ga_{0.3}As$ MOSFET with spin-polarized carriers is explored using ensemble MC device simulations. We report on the behaviour of spin polarization, both its magnitude and polarization angle relative to the initial polarization vector, as a function of temperature (300 K–77 K) while varying device lateral geometry. Specifically, the effects of varying the gate lengths, and the source-to-gate and the gate-to-drain spacers on both the magnitude and the angle of the spin polarization vector are studied.

The simulation results for the temperature dependence show that the magnitude of the spin polarization in the drain region increases with decreasing temperature. However, decreasing the temperature also reduces the Rashba coupling and the degree of rotation the polarization vector undergoes as the spin-polarized electrons travel through the channel. Combining these effects show that the spin modulation, which quantifies the modulation of the drain current due to the spin–orbit coupling, actually increases with increasing temperature.

Our simulation results show that increasing the gate and spacer lengths (within realistic limits) is either neutral or increases the magnitude of the spin polarization at the drain edge due to the refocusing effect [24], which is enhanced when the gate or the spacer lengths increase, although this enhancement is limited to the nanoscale dimensions of the device. This increase in the spin polarisation is inconsistent with a simple model, which would suggest that increasing the gate length and, especially, the spacer lengths should decrease the

magnitude of the spin polarization at the drain edge due to the increased channel length resulting in a greater depolarization. Beyond that, the simple model predicting a decrease of the spin polarization at the drain edge becomes valid.

While it remains to be seen what architectures are ultimately best for spin-FETs and spintronics applications, the results presented on spin transport and control mechanisms in realistic systems can be utilized to develop new designs for spin applications that properly take into account trade-offs such as increased spin polarization and injection efficiency vs. reduced polarization control at lower temperatures, and optimize controllable design parameters such as channel and spacer lengths to maximize spin-refocusing effects. Although the simulations are limited to a particular design of an InGaAs FET, spin refocusing effects play an important role in NMR and ESR, and if they could be exploited in semiconductor spin-FET designs, this might lead to more practical and functional designs for new applications.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgements

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Appendix A. Parameters used for temperature dependence of band energies

Table A1 summarises fitting material parameters for GaAs, InAs, and $In_{0.3}Ga_{0.7}As$ used in the calculations of band energies.

Table A1. Fitting parameters as bandgap E_{g0}, θ, and α_B used to obtain the temperature dependent band energies and Kane parameters. E_0 and E_1 are the zero and the first energy bands (the zero energy is set to the bottom of the conduction band), Δ_0 and Δ_1 are the zero and the first spin-orbit splitting energies, P_0 and P_1 are the optical matrix elements for the zero and the first energy bands. P_0 and P_1 are assumed to be temperature independent for InAs and $E_{0/1} + \Delta_{0/1}$ has the same temperature dependence as $E_{0/1}$.

	GaAs[a]			InAs			$In_{0.3}Ga_{0.7}As$		
Parameter	E_{g0}(eV)	α_B(meV)	θ(K)	E_{g0}(eV)	α_B(meV)	θ(K)	E_{g0}(eV)	α_B(meV)	θ(K)
E_0	1.571	57	240	0.414[b]	28.10[b]	147[b]	1.224	48.30	212.10
E_1	4.456	59	323	4.453[c]	41.00[c]	262[c]	4.455	53.60	304.70
$E_0 + \Delta_0$	1.907	58	240	0.807[b,d]	28.10[b,d]	147[b,d]	1.577	49.03	212.10
$E_1 + \Delta_1$	4.659	59	323	4.936[e]	64.00[e]	159[e]	4.742	60.50	273.80
$2P_0^2/\hbar^2$	30.58	1040	240	—	—	—	—	—	—
$2P_1^2/\hbar^2$	8.84	1040	240	—	—	—	—	—	—

[a] Hubner *et al* [38].
[b] Passler [41].
[c] Kim *et al* [47].
[d] Assumed to have the same dependence as E_0 due to lack of data.
[e] Kim *et al* [40].

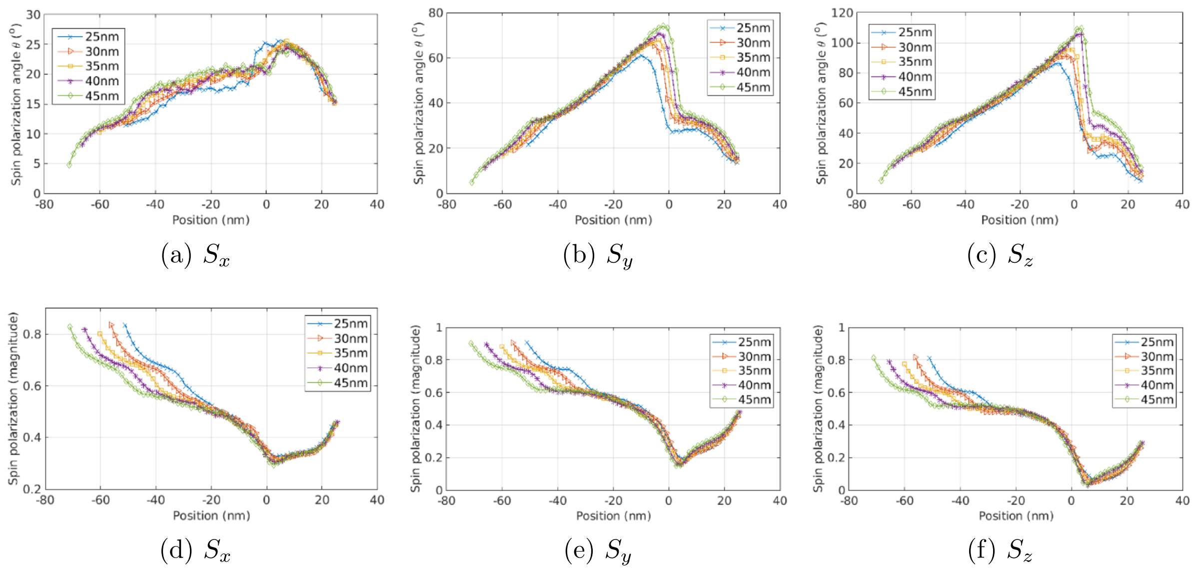

Figure B1. A spin polarization angle and a magnitude of the spin polarization for the *x*, *y*, and *z* components as function of the position along the channel for the different gate lengths.

Appendix B. Auxiliary figures

Figures B1–B3 plot a spin polarization angle θ and a magnitude of spin polarization along the device channel at a drive voltage (a gate voltage of 0.9 V, a drain voltage of 0.7 V) for different gate lengths, source-to-gate spacers, and gate-to-drain spacers, respectively.

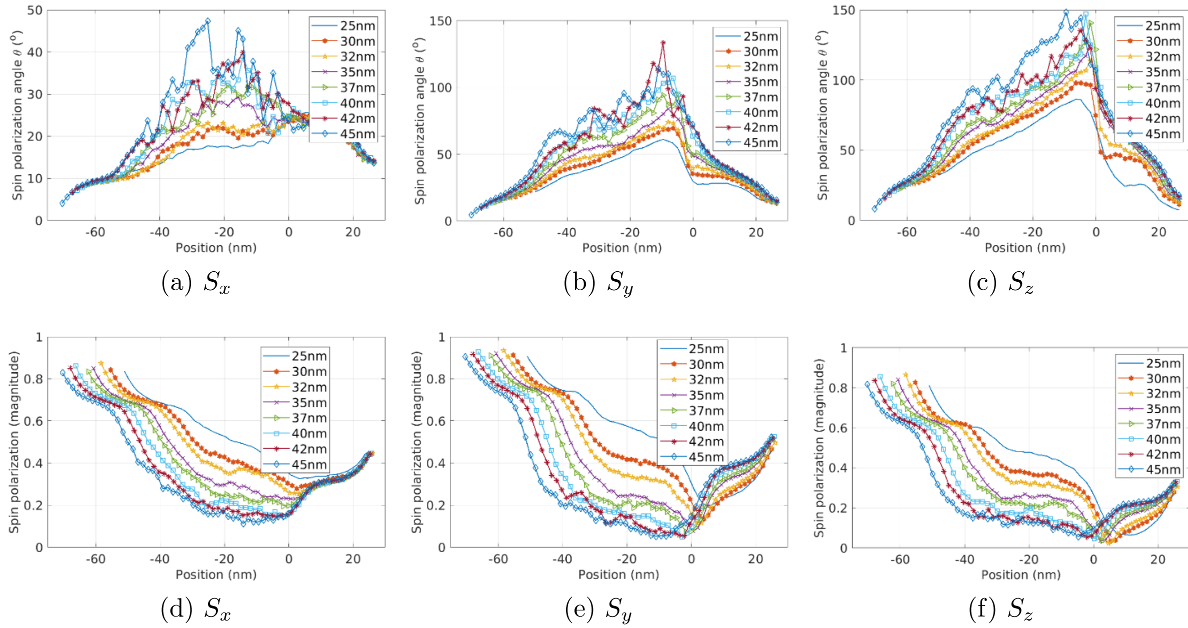

Figure B2. A spin polarization angle and a magnitude of the spin polarization for the *x*, *y*, and *z* components as function of the position along the channel for the different source-to-gate spacer lengths.

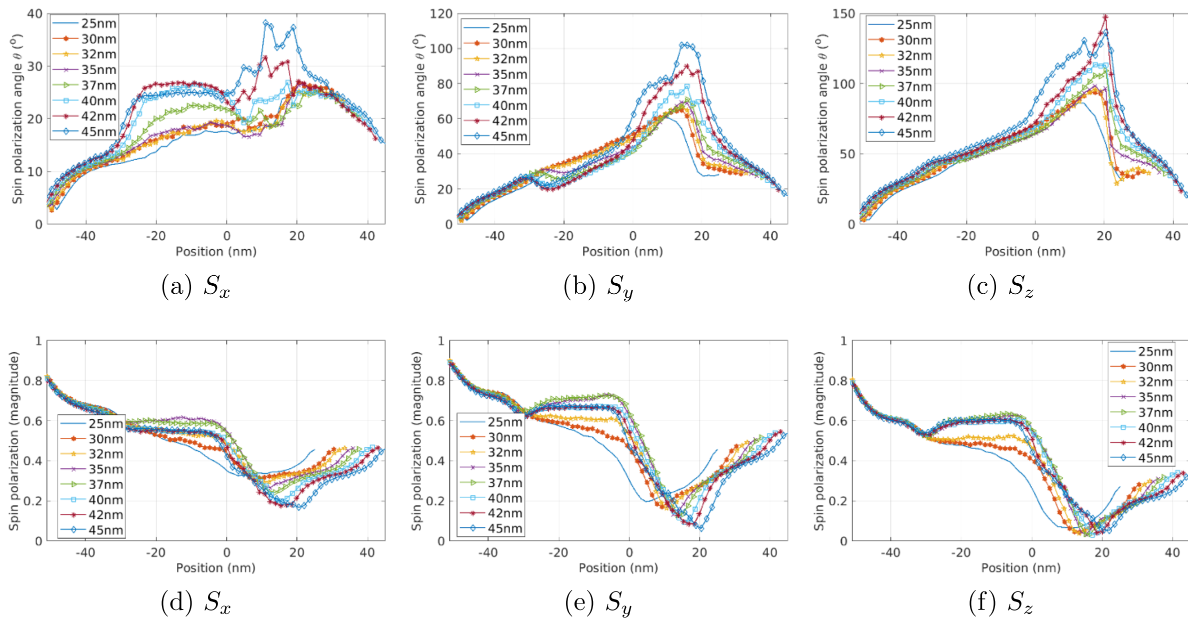

Figure B3. A spin polarization angle and a magnitude of the spin polarization for the *x*, *y*, and *z* components as function of the position along the channel for the different gate-to-drain spacer lengths.

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