# Interfaces and Junctions in Nanoscale ZnO and InAs Transistor Structures

**Mohamed, Alnazer**

Prifysgol Abertawe
Swansea University

# Interfaces and Junctions in Nanoscale ZnO and InAs Transistor Structures

Alnazer Mohamed

Submitted to Swansea University in fulfilment of the requirements for the degree of Doctor of Philosophy

Swansea University
February 2019

# Declaration of authorship

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.
Signed ..... (candidate)
Date .....

This thesis is the result of my own investigations, except where otherwise stated. Where correction services have been used, the extent and nature of the correction is clearly marked in a footnote(s).
Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

Signed ..... (candidate)
Date .....
I hereby give consent for my thesis, if accepted, to be available for photocopying and for inter-library loan, and for the title and summary to be made available to outside organisations.

Signed ..... (candidate)
Date .....

**Abstract**

In this thesis, a multi-scale simulation study of Ni/InAs nano-scale contact aimed for the sub-14 nm technology is carried out to understand material and transport properties at a metal-semiconductor interface. The deposited Ni metal contact on an 11 nm thick InAs channel forms an 8.5 nm thick InAs leaving a 2.5 nm thick InAs channel on a *p*-type doped ($1\times10^{16}$ cm$^{-3}$) $AlAs_{0.47}Sb_{0.53}$ buffer. The density functional theory (DFT) calculations reveal a band gap narrowing in the InAs at the metal-semiconductor interface. The one-dimensional (1D) self-consistent Poisson-Schrödinger transport simulations using real-space material parameters extracted from the DFT calculations at the metal-semiconductor interface, exhibiting band gap narrowing, give a specific sheet resistance of $R_{sh} = 90.9$ Ω/sq which is in a good agreement with an experimental value of 97 Ω/sq.

In this thesis, ZnO thin-film transistors (TFTs) with different channel lengths (10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m) have been characterised. The current-voltage measurements indicate *n*-type channel, enhancement mode TFT operation with an excellent drain current saturation. A transmission line method (TLM) is employed to extract the contact resistance, effective and channel electron mobility from current-voltage characteristics in the linear regime of transistor operation. Contact resistance and both effective and channel electron mobility exhibit a dependency on the channel length as a function of gate bias (10 V and 15 V). The extracted channel electron mobility is high as 0.782 cm$^2$/Vs and 0.83 cm$^2$/Vs (increase by 6 %) at gate biases of 10 V and 15 V, respectively, for the 10 $\mu$m channel length as compared to effective mobility of 0.11 cm$^2$/Vs and 0.38 cm$^2$/Vs, at the same respective biases.

The channel mobility increases from 8.9 cm$^2$/Vs to 19.04 cm$^2$/Vs (increase by 115 %) when gate biases increases from 10 V and 15 V, respectively, when the channel length is scaled down to 2 $\mu$m. The increase of the electron channel mobility during the channel scaling is indicative of a reduced electron scattering due to the increase in electric field along the channel. This reduction in the carrier scattering increases electron velocity because electrons will have a longer mean-free path in the scaled thin-film channels. These values indicate a substantial increase in ZnO TFTs electron mobility as compared to previously reported values for such devices.

In addition, ZnO NWs field-effect transistors (NWs-FETs) fabricated by using top-down fabrication have been studied. The top-down fabrication method starts with a thin film deposition by remote plasma enhanced ALD (PEALD). The PEALD is followed by aniso-tropically reactive ion etch (RIE) to produce ZnO NWs with different channel lengths (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m). Optical and electrical characterisations are carried out to study the impact of scaling channel length ($L_{ch}$) in the transistors.

**Acknowledgements**

My sincere gratitude to my supervisor Dr. Karol Kalna. This work would not has been possible without his support and helps. His guidance, patience, motivation, immense knowledge, the continuous support and taught me a great deal about both scientific research and life in general during my Ph.D. I am especially indebted to express my thankful to my supervisor, Dr. Richard J. Cobley who have been supportive during my PhD journey and who worked actively to provide me with the protected academic time to pursue this goal.

I am extremely thankful to my dear father (Hamed), who is passed away last March, for his numerous sacrifices he made for my brothers and I.

This thesis is dedicated to him for all his love and support since my childhood until his last breath. May God forgive him, elevate his status among the guided people, and comfort him in his grave, lighten his stay (in the grave), and may God grant and dwell him beautiful paradise. May he make his grave a place of comfort and light. May God make him pass successfully in all the stages of the life after death.

Nobody has been more important to me in the pursuit of this project than the members of my family. I would like to thank my mother whose love and guidance is with me in whatever I pursue. My dear beloved mother, has been a constant source of support and encouragement, she is made an speakable number of sacrifices for the entire family, and specifically for me to continue my schooling. She is a great inspiration to me. My great appreciation and enormous thanks for her.

I wish to thank all my siblings, who are provide unending inspiration, and playing a great part in my life.

Special mention goes to Southampton Nanotechnology Centre, School of Electronics and Computer Science at the University of Southampton for going far beyond the fabrications and sample prepare. To Dr. Harold M. H. Chong, for advising, and for providing with a fantastic knowledge and information. Special thanks to Mrs. Azlin Ghazali, for preparing and fabricating the samples.

Similar, I am particularly indebted to Naif Alshehrifor his constant faith and for his support in my scan electron microscope.

Besides my supervisors, I would like to thank the rest of my colleagues and mentors, Dr. Manuel Aldegunde, Dr. Richard Oxland, Dr. Steven Hepplestone, Dr. Peter Sushko and Dr. Chris Barnett for their insightful comments and encouragement to widen my research from various perspectives.

I am grateful to all of those with whom I have had the pleasure to work during my PhD, my research group, each members has provided me an extensive personal and professional guidance for the stimulating discussions and for all the fun we had.

# List of contributions

## Journal publications

**A. H. Mohamed**, R. Oxland, M. Aldegunde, S. P. Hepplestone, P. V. Sushko, and K. Kalna, "Narrowing of Band Gap at Source/Drain Contact Scheme of Nanoscale InAs-nMOS", *Solid State Electronics*, vol. 142, pp. 31-35, Apr. 2018.

## Conferences

**A. H. Mohamed**, H. M. H. Chong, and K. Kalna,"Effective and Channel Mobility Extraction for ZnO Thin-Film Transistors", *3rd NANOENERGY 2016*, Liverpool, July 2016 (Oral).
**A. H. Mohamed**, H. M. H. Chong, and K. Kalna, "Electron Mobility Extraction in ZnO Nanowire FETs by a Top-Down Approach", *42nd Micro and Nano Engineering (MNE2016)*, Austria, July 2016 (Poster).
**A. H. Mohamed**, H. M. H. Chong and K. Kalna, "Effective and Channel Mobility Extraction in ZnO Nanowire Transistors", *UK Semiconductors*, Sheffield, June 2016 (Poster).
**A. H. Mohamed**, M. A. Elmessary, M. Aldegunde, D. Nagy, and K. Kalna, "Bandgap Narrowing of Metal Semiconductors Contact", *UK Semiconductors*, Sheffield, July 2015 (Poster).
**A. H. Mohamed**, D. Nagy, M. Aldegunde, and K. Kalna, "An Approach Model to Study Ultra-low Resistance Source-Drain contact of n-MOS", *28th International Conference on Defect in Semiconductors*, Espoo, Finland, July 2014 (Oral).

## In-house Conferences

**A. H. Mohamed**, M. A. Elmessary, D. Nagy, M. Aldegunde, and K. Kalna, "The Impact of Band Gap Narrowing on Metal Semiconductors contacts", *ESDC*, Swansea University, December 2014 (Oral).
**A. H. Mohamed**, M. Aldegunde, M. A. Elmessary, D. Nagy, and K. Kalna, "InAs Source Drain Contact Resistance", *ZC2E*, Swansea University, January 2015 (Poster).
**A. H. Mohamed**, M. A. Elmessary, D. Nagy and K. Kalna, "Electron Mobility Extraction for ZnO-TFt-FETs by a Top-Down Approach",*ZC2E*, Swansea University, January 2015 (Poster).
**A. H. Mohamed**, R. J. Cobley, and K. Kalna, "Electrical Characterisation of ZnO-TFTs", *ZC2E*, Swansea University, September 2016 (Poster).

# Contents

**Contents** i

**List of Tables** xi

**1 Introduction** 1
- 1.1 Introduction . . . 1
- 1.2 Research Aims and Objectives . . . 2
- 1.3 Thesis Outline . . . 3

**2 Theoretical Background** 7
- 2.1 Introduction . . . 7
- 2.2 Energy Band Structure . . . 9
- 2.3 Band Gaps For The Doped Semiconductors . . . 10
- 2.4 Metal Work Function . . . 11
- 2.5 Schottky Barrier Height . . . 11
- 2.6 Ohmic Contact . . . 12
- 2.7 Current Transport Mechanisms . . . 13
- 2.8 MOSFET Physics . . . 14
  - 2.8.1 Scaling Theory . . . 16
  - 2.8.2 Short Channel Effects . . . 17
  - 2.8.3 Threshold Voltage and Sub-Threshold Current . . . 20
  - 2.8.4 Drain Induced Barrier Lowering . . . 20
  - 2.8.5 Back Gate in Transistor . . . 21
- 2.9 Transmission Line Method . . . 22
- 2.10 Effective Electron Mobility . . . 24
- 2.11 ZnO Properties and Structure . . . 26
  - 2.11.1 ZnO Crystal Structural and Chemical Binding . . . 26
  - 2.11.2 ZnO Physical Properties . . . 27
  - 2.11.3 ZnO Electronic Band Structure . . . 28
  - 2.11.4 ZnO Optical and Transitions Properties . . . 29
  - 2.11.5 Defects and Emission Properties of ZnO . . . 30
- 2.12 Synthesis of ZnO . . . 30
  - 2.12.1 Bottom-up Process . . . 30
  - 2.12.2 Top-Down Process . . . 32
  - 2.12.3 ZnO Film Deposition . . . 33
  - 2.12.4 ZnO Thin Film Transistors . . . 34
  - 2.12.5 ZnO Nanowire Field-Effect Transistors . . . 34
- 2.13 Conclusion . . . 36

**3 Methodology and Characterisation Techniques** 45

3.1 Introduction . . . 45
3.2 CVD Grow and Reaction Set-Up . . . 45
3.2.1 Reactant Transport . . . 47
3.2.2 Chemical Vapour Deposition Reactors . . . 47
3.2.3 Substrate Loading Mechanism . . . 49
3.2.4 Energy Source . . . 50
3.2.5 Vacuum System . . . 50
3.2.6 Exhaust System . . . 51
3.2.7 Growth Rate . . . 51
3.2.8 Nucleation Growth . . . 52
3.2.9 Film Deposition . . . 53
3.2.10 The Key Growth Parameters Affecting Domain Structure of CVD . . . 54
3.3 Experimental Techniques . . . 54
3.3.1 Scanning Electron Microscope . . . 54
3.3.2 Energy Dispersive X-Ray . . . 55
3.3.3 X-Ray Photo-electron Spectroscopy . . . 57
3.3.4 Photo-luminescence . . . 59
3.3.5 Four point probes measurement . . . 60
3.4 Conclusion . . . 61

**4 Simulation Results and Discussion-Source/Drain Contact of Nano-Scale InAs nMOS 65**
4.1 Introduction . . . 65
4.2 Nickel Contact for Source/Drain of III-V MOSFET . . . 66
4.3 Density Functional Theory Calculations of the Structure . . . 67
4.3.1 Transport Through Contact and Carrier Transport Equations . . . 68
4.3.2 Solving Schrödinger Equation . . . 70
4.3.3 Solving Poisson Equation . . . 73
4.3.4 Self-Consistent Solution of Schrödinger-Poisson Equations . . . 75
4.4 Material Parameters . . . 75
4.4.1 Band Gap Energy . . . 75
4.4.2 Band Gap Offset . . . 79
4.4.3 Effective Mass . . . 79
4.5 Schottky Barrier Hight and Metal Work Function . . . 82
4.6 Electron Mobility . . . 83
4.7 1D Transport Simulations . . . 83
4.8 Band Gap Narrowing . . . 84
4.9 Source-Drain Series Resistance . . . 85
4.10 Conclusion . . . 87

**5 Top-Down Fabrication of ZnO Devices, Characterisation Results, Analysis and Discussion 91**
5.1 Introduction . . . 91

5.2 ZnO TFTs Fabrication . . . 93
5.2.1 Remote Plasma Enhanced Atomic Layer Deposition . . . 93
5.2.2 Top-Down Fabrication of ZnO TFTs . . . 93
5.3 Electrical Characterisation of ZnO TFTs . . . 94
5.3.1 Output Characteristics of ZnO TFTs . . . 95
5.3.2 Breakdown Voltages of ZnO TFTs . . . 95
5.3.3 The Effect of Channel Length Scaling on Current, Threshold and Sub-Threshold Regions of ZnO TFTs . . . 97
5.3.4 Drain Induced Barrier Lowering of ZnO TFTs . . . 99
5.3.5 Total Resistance with Scaled Channel Length of ZnO TFTs . . . 99
5.3.6 Contact Resistance of ZnO TFTs . . . 103
5.3.7 Effective Mobility of ZnO TFTs . . . 104
5.3.8 Channel Mobility of ZnO TFTs . . . 106
5.4 ZnO NW-FETs Fabrication . . . 109
5.4.1 Remote Plasma Enhancement Atomic Layer Deposition . . . 109
5.4.2 Top-Down Fabrication of ZnO NW-FETs . . . 110
5.5 Electrical and Optical Characterisation of ZnO NW-FETs . . . 113
5.5.1 Optical Properties of ZnO NW-FETs . . . 113
5.5.2 Output Characteristics of ZnO NW-FETs . . . 114
5.6 Transfer Characteristics of ZnO NW-FETs . . . 116
5.6.1 Impact of Channel Length on Threshold Voltage of ZnO NW-FETs . . . 117
5.7 Conclusion . . . 120

**6 Conclusion and Future Work** **125**
6.1 Conclusion . . . 125
6.2 Proposal for Future Work . . . 126

# List of Figures


1.1 Schematic illustrating the layout of chapters in this thesis. . . . . 5

2.1 (a) Perspective view of metal semiconductor contact, (b) energy band gap diagram of metal-semiconductor junction, where $\Phi_M$ is the metal work function, $\phi_S$ is the Schottky barrier height, $E_F$ is the Fermi level, $\chi$ is the electron affinity, $E_C$, $E_V$ are the conduction and valence bands, respectively. . . . . 8

2.2 Electronic band structures of metals, semiconductors and insulators. . 9

2.3 (a) $n$-type metal-semiconductor band gap diagram, (b) $p$-type metal-semiconductor band gap diagram. . . . . 10

2.4 (a) Band gap diagram of InAs semiconductors and metal work function for some material. (b) Schematic shows the metal work function definition. . . . . 12

2.5 Band gap structure of metal-semiconductor contact at thermal equilibrium. . . . . 13

2.6 Current-voltage characteristics of (a) an Ohmic contact and Schottky contact of a metal-semiconductor interface, (b) the energy alignments of the metal contacting with a semiconductor in the case of the Ohmic contact. . . . . 14

2.7 Transport mechanisms at metal-semiconductor junctions. . . . . 15

2.8 (a) Cross section of $n$-channel MOSFET structure. (b) Transistor operation modes of a typical $n$-channel enhancement mode MOSFET. 16

2.9 The trend in MOS channel length scaling and the prediction made in the 2003 International Technology Roadmap for Semiconductors [9]. . 18

2.10 The top schematics show a cut of long-channel (dashed line) and short channel (solid line) MOSFETs. The bottom schematics show the change in potential barrier profile along the surface of the channel (from the source to the drain). The dash line shows the potential barrier along the channel in a long-channel MOSFET while the solid line show the movement/decrease of the potential barrier along the channel in a short-channel MOSFET. On the left side, $V_D$=0, while on the right side, the drain voltage is large to show the DIBL effect [22]. 21

2.11 Schematic illustrates $n$ type Si-FET backed gate. . . . . 22

2.12 Schematic diagram shows the TLM structure. . . . . 24

2.13 An example of a plot of total resistance as a function of TLM pad spacing. . . . . 25

2.14 Schematic diagram of a field-effect transistor to extract the channel current and electron mobility. . . . . 26

2.15 (a) ZnO wurtzite structure blue and green planes represent the rows of Zn and O charged planes. Red is reserved for O, Gray for Z [34]. (b) The wurtzite unit cell of a non-centre symmetric structure. (c) Various crystal planes of ZnO wurtzite structure show the hexagonal each anion of ZnO surrounded by four cations. . . . . 27
2.16 Calculated band structure of wurtzite ZnO using a local-density approximation [30]. . . . . 29
2.17 A schematic showing the defect types in crystal structure. . . . . 31
2.18 (a) Scanning electron microscopy image of ZnO NWs synthesized by a vapour liquid solid (VLS) method [49]. (b) Scanning electron microscopy of a dense carpet of ZnO NWs after a hydrothermal growth. (c) Transmission electron microscopy image of one of ZnO NWs grown by a hydrothermal growth. The inset confirms the single crystalline structure of the ZnO NWs. (d) Atomic force microscopy image of an as-grown NWs with Al source and drain contacts [47]. . . . . 32
2.19 SEM image of ZnO nanowire array fabricated by a top-down fabrication method [45]. . . . . 33

3.1 Schematic diagram of CVD apparatus. Reaction gas is supplied on one end of the apparatus, and gas outlet on the other end. . . . . 46
3.2 Schematic shows the hot wall CVD reactor. . . . . 48
3.3 Schematic shows the cold wall CVD reactor. . . . . 50
3.4 Arrhenius plot of the dependence between CVD deposition rate and temperature. . . . . 52
3.5 Precursor transport, nucleation growth and reaction processes in CVD. 53
3.6 (a) Shows a schematic diagram of the fundamental components of SEM. (b) The basic process of SEM steps [17]. . . . . 56
3.7 Schematic diagram shows an atoms core shells and basic principles of EDX [15]. . . . . 57
3.8 Schemes for (a) soft X-ray emission spectroscopy showing the atomic orbital distribution inside the molecules and (b) soft X-ray photoelectron spectroscopy of sample showing the binding energy exhibiting a set of peaks depended on kinetic energy in the XPS spectrum. . . . 59
3.9 (a) A photo-luminescence based contact-less gas sensing set-up, (b) energy diagram showing absorption of light and the processes involved in the emission of light as fluorescence and phosphorescence. . . . . 59
3.10 (a) Four point probe system, (b) schematic diagram of equivalent circuit of a four-point probe connected to three terminals. . . . . 60

4.1 Schematic of layer structure for MOSFET. Structure has an 8.5 nm $Ni_3InAs$/2.5 nm InAs and $AlAs_{0.47}Sb_{0.53}$ layers. The $Ni_3InAs$ alloy is formed by Ni deposition on the 10 nm InAs layer. . . . . 66
4.2 (a) The layered projected density of states (LPDOS) for the $Ni_3InAs$/InAs interface calculated using VASP. (b) Atomic structure for $Ni_3InAs$/InAs from Ref. [10]. . . . . 68
4.3 Band diagram of the single-heterojunction and the bounded state wave function of GaAs and AlGaAs. The structure shows the discretization of the potential using a non-uniform mesh simulation [11]. 71

4.4 Flowchart shows the approach of solving the Schrödinger-Poisson system self-consistently in an iterative process. . . . . 76
4.5 Conduction and valence band edges as a function of the position (continuous red line) and extracted from the DFT calculations (black diamonds) of GaAs. Fermi level (dashed black line) is set at 0 eV [10]. . 77
4.6 Band gaps $E_g^{\Gamma}$, $E_g^{x}$, $E_g^{L}$ and electron affinity $\chi$ on the composition $x$ [13]. . . . . 78
4.7 The schematic showing the energy band gap diagram between AlAs and AlSb. . . . . 79
4.8 Band diagrams for the heterojunction by Anderson's rule. The junction alignment at equilibrium (bottom) is predicted based on flat vacuum alignment (top). . . . . 80
4.9 The computed dependences of electron effective masses $m^*$ on the concentration x for $AlAs_{0.47}Sb_{0.53}$ alloys [13]. . . . . 82
4.10 Electron mobility vs. applied electric field in bulk InAs obtained from ensemble Monte Carlo simulations [21]. . . . . 84
4.11 Conduction and valence band profiles at equilibrium of the InAs (8.5 nm)/ InAs (2.5 nm)/$AlAs_{0.47}Sb_{0.53}$ heterostructure assuming a constant band gap at the interface for Schottky barrier height of (a) 0.11 eV and (b) 0.30 eV. . . . . 85
4.12 (a) Conduction and valence band profiles for Ni/InAs (8.5 nm)/InAs (2.5 nm)/$AlAs_{0.47}Sb_{0.53}$ (960 nm) heterostructure assuming the band gap narrowing and a SBH of 0.11 eV at equilibrium. The energies for the band gap narrowing of InAs at the interface from the DFT are: $\Delta E_G$ (0.2 nm) = 0.354 eV, $\Delta E_G$ (0.4 nm) = 0.204 eV, $\Delta E_G$ (0.6 nm) = 0.254 eV, $\Delta$ E $_G$ (0.8 nm) = 0.304 eV, $\Delta E_G$ (1.0 nm) = 0.354 eV. (b) The constant band gap for a SBH of 0.30 eV. The band gap narrowing of InAs at the interface follows the same steps as in (a). . . . . 86
4.13 Sheet resistance for InAs (8.5 nm)/InAs (2.5 nm)/$AlAs_{0.47}Sb_{0.53}$ (960 nm) contact heterostructure as a function of metal work function (Ni) comparing simulations using the same band gap in whole InAs and with those when the band gap narrowing towards metal-semiconductor interface is accounted for. The experimental value of sheet resistance [3] is shown by green triangle. . . . . 86

5.1 Top-down fabrication process of ZnO TFTs (a) $SiO_2$ thermally grown through wet oxidation 200 nm and $SiO_2$ dry thermal oxidation in the RIE to form a trench. (b) ZnO thin film deposited by the remote plasma. (c) Schematic structure of ZnO thin-film FET fabricated by using top-down fabrication method via remote plasma atomic layer deposition (ALD). . . . . 92
5.2 SEM images of ZnO TFTs with the Al pad which serves as contacts. 94
5.3 Output ($I_D$-$V_D$) characteristics from $V_G$ = 20 V to 2 V with a step of 2 V for ZnO TFTs with different channel lengths ($L_{ch}$) of (a) 10 $\mu$m, (b) 5 $\mu$m, (c) 4 $\mu$m, and (d) 2 $\mu$m, respectively. . . . . 96
5.4 Output $I_D$-$V_D$ characteristic of a ZnO TFTs with a channel length $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m exhibiting a breakdown voltage 79.91 V, 70.07 V, 64.68 V, and 58.85 V, respectively. . . . . 97

5.5 Transfer $I_D$-$V_G$ characteristics under a drain bias of $V_D$ = 5.0 V for (a) 10 $\mu$m, (b) 5 $\mu$m, (c) 4 $\mu$m, and (d) 2 $\mu$m channel length ZnO TFTs, respectively. . . . . 98
5.6 Extraction of DIBL from the drain current versus the gate voltage ($I_D$-$V_G$) characteristics of ZnO TFTs with different channel lengths of (a) $L_{ch}$ = 10 $\mu$m, (b) $L_{ch}$ = 5 $\mu$m, (c) $L_{ch}$ = 4 $\mu$m, and (d) $L_{ch}$ = 2 $\mu$m.100
5.7 The DIBL of ZnO TFTs shows the increase with the decrease in channel lengths of $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m. . . . . 100
5.8 Total resistance for (a) the 10 $\mu$m ZnO TFT channel length, (b) the 5 $\mu$m ZnO TFT channel length, (c) the 4 $\mu$m ZnO TFT channel length, and (d) the 2 $\mu$m ZnO TFT channel length under a gate bias of $V_G$ = 10.0 V. . . . . 102
5.9 Normalised total resistance versus the channel length, $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m, at gate biases of $V_G$ = 10.0 V and 15.0 V. The dash lines are guide to the eyes. . . . . 102
5.10 Contact resistance versus the gate voltage at different gate bias ($V_G$= 10.0 V and 15.0 V). . . . . 104
5.11 Effective electron mobility extracted using. The electron mobility decreases with increasing of the channel length at $V_G$=10.0 V and 15.0 V. . . . . 107
5.12 Channel electron mobility extracted using Eq. (5.14), channel mobility shows that increasing rapidly with increased channels length at gate biases of $V_G$ = 10.0 V and 15.0 V. . . . . 109
5.13 Top-down fabrication process of ZnO NW-FETs, (a) a *p*-type silicon wafer as a substrate and a dry thermal oxidation grow of 100 nm $SiO_2$ layer, (b) photo-lithography and anisotropic RIE to form a 100 nm trench, (c) ZnO thin film deposited by a remote plasma and dry etched to form the NWs, and (d) final fabricated ZnO NW-FETs. . . 111
5.14 Schematic illustration of the top-down fabrication process of ZnO NW-FETs. The inset shows the SEM of the two identical NWs across the Al pad. . . . . 112
5.15 (a) Optical microscope views a pair of ZnO NWs in contact with Al pad. (b) Optical image of two NWs with an approximative height of 80 nm. This value was determined by the height of the $SiO_2$ pillar and the amount of over-etch of the ZnO layer. (c) A pair of NWs from SEM after the RIE etch. . . . . 113
5.16 SEM cross-sectional view of ZnO NWs fabricated on a $SiO_2$/Si substrate with (a) a channel length of 20 $\mu$m with 2 NWs, (b) a channel length of 10 $\mu$m with 16 NWs, and (c) a channel length of 10 $\mu$m with 2 NWs, and (d) a channel length of 2 $\mu$m with 2 NWs. . . . . 114
5.17 Transfer $I_D$-$V_G$ characteristics under a drain bias of $V_D$ = 5.0 V for the ZnO NWs with different channel lengths $L_{ch}$ of (a) 20 $\mu$m (2 NWs), (b) 10 $\mu$m (16 NWs), (c) 10 $\mu$m (2 NWs), and (d) 2 $\mu$m (2 NWs), respectively. . . . . 115
5.18 Output $I_D$-$V_D$ characteristics from $V_G$ = 40.0 V to 2.0 V with a step of 2.0 V for the ZnO NWs with a channel length $L_{ch}$ of 2 $\mu$m (2 NWs).116
5.19 Transfer ($I_D$- $V_G$) characteristics under a drain bias of $V_D$= 1.0 V and 5.0 V for different channel lengths of $L_{ch}$ = 2 $\mu$m (2 NWs), 10 $\mu$m (2 NWs), 10 $\mu$m (16 NWs) and 20 $\mu$m (2 NWs). . . . . 119

5.20 Variation of threshold voltage $V_{Th}$ as a function of the channel length. Figure shows the dependence between threshold voltage and channel length at different drain biases of 1.0 V (red stars) and 5.0 V (black circles). . . . . 119

6.1 Illustration of the work demonstrated in this thesis. . . . . 127

# List of Tables


2.1 Classical MOSFETs scaling parameters versus the scaling factor of each parameter. . . . . 17
2.2 The basic physical parameters of ZnO. . . . . 28
2.3 Survey of various ZnO thin film deposition techniques, and the extracted mobility demonstrated by different research groups. . . . . 35
2.4 Review of ZnO NWFET electrical performance. . . . . 36

4.1 Energy band parameters: InAs, AlAs, AlSb and $AlAs_{0.47}Sb_{0.53}$. . . . . 78
4.2 InAs, $Ni_3InAs$ and $AlAs_{0.47}Sb_{0.53}$ material and structure parameters from literature used in a modelling of the Al $As_{0.47}Sb_{0.53}$ contact, electron mobility has been obtained from Monte-Carlo simulation as it shows in Fig. 4.10. . . . . 81
4.3 Sheet resistance of nanoscale metal contact for several combination of parameters. . . . . 83

5.1 Extracted breakdown voltage versus channel length for 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m. . . . . 96
5.2 Effective electron mobility extracted using Eq. (5.8), mobilities are decrease with channel lengths ($L_{ch}$) of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m increased at two different gate biases of $V_G$ = 10 V and 15 V. . . . . 106
5.3 Channel resistance extracted using Eq. (5.1), channel resistances are increasing with channel lengths ($L_{ch}$) of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m increased at two different gate biases of $V_G$ = 10.0 V and 15.0 V. . . 108
5.4 Channel electron mobility extracted using Eq. (5.14), mobilities are increasing rapidly with channel lengths ($L_{ch}$) of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m increased at two different gate biases of $V_G$ = 10.0 V and 15.0 V. . . . . 108
5.5 The impact of threshold voltage on a channel length at different gate biases of $V_D$=1 V and 5 V. . . . . 118

# Chapter 1

# Introduction

## 1.1 Introduction

Metal-semiconductor junctions are playing an increasingly important role in nanoscale manufacturing of semiconductor devices [1]. The critical issue for these junctions is the interface between metal and semiconductor which quality is essential to maintain in order to manufacture novel nano-scale devices [2]. A major current trend in the semiconductor industry is a shift into new materials that help to deliver new functionality or improve performance in applications [3].
The main challenges for interface technology are:

i. The interface between metal and semiconductor for a low contact resistance and a high mobility in the range of nanoscale.

ii. The range of operation and stability at nanoscale for these devices [4].

Introducing new devices with a small dimensions brings many benefits such as increased performance and improved operation of semiconductor devices, a new functionality offered by semiconductor devices, and a reduced cost for companies and users [3]. However, introducing a new technique to down scale electronic devices becomes more challenging. The scale down electronic devices require a functioning interface between a metal and a semiconductor. These materials are often synthesized and processed using different techniques and under different conditions such as the composition of the semiconductors GaAs, InAs, InP, GaN, AlSb, ZnO, AlAs etc. [5].
Among the II-V and III-V semiconductor, zinc oxide (ZnO) has been extensively

studied for their abundant physical properties and versatile device applications [6]. The ZnO structures of low dimensions ($\sim$ 100 nm) represent an ideal case for scientific research regarding to the fundamental properties such as charge transport, spin transport, light coupling, piezoelectric and magnetic properties [7]. ZnO have demonstrated a very unique remarkable characteristics due to their anisotropic geometry and size [8]. The ZnO with a very small diameter ($<$ 100 nm) have shown a sensitive superior performance to the chemical interactions [9]. ZnO thus has become a cutting edge of nanotechnology research in opto-electronics, transparent electronics, and sensors [10]. intensively ZnO, researched as an alternative channel material for semiconductor field effect transistors (FETs) due to its acceptable material properties (a wide band gap of 3.37 eV and an electron mobility in the range of 1-100 $cm^2/Vs$ at room temperature) [8]. A major advantage of use of ZnO in manufacturing is its very low cost, a low temperature processing, and the ZnO environmental friendliness. ZnO is also considered as one of the most promising semiconductor materials for complementary metal oxide semiconductors (CMOS) [11].

## 1.2 Research Aims and Objectives

The aims and objectives of this thesis are:

I. Overview the interface between metal-semiconductor junctions at nano-scale dimensions, the study investigate the electrical and optical properties by looking at different types of materials such as ZnO, Si, $Sio_2$ InAs, NiInAs, and AlAsSb and the interfaces between these materials.

II. A multi-scale simulation study of a nano-scale contact combining the density functional theory (DFT) calculations with the solution of 1-dimensional Schrödinger-Poisson (1DSP) equation. The simulation aims to understand a relation among a contact resistance and a narrowing of band gap in semiconductor at the interface of the source/drain contact in a nano-scale InAs nMOS and an overview of the semiconductor theory with emphasis on Schottky contacts relevant to the future of sub-10 nm technology.

III. Study ZnO thin-film transistors (TFTs) and ZnO nanowire field-effect transistors (NW FETs) with a different channel lengths grown by a top-down fabrication (via remote plasma atomic layer deposition). The study undergone

through electrical characteristics of ZnO TFTs with channel lengths (10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m) and analyse the effects of statistical variability on threshold voltage $V_{Th}$ and DIBL.

IV. Demonstrate and perform the electrical measurements of ZnO thin-film transistors (TFTs) using transmission line method (TLM) to obtain the contact resistance and calculate effective and channel mobility in the devices with different channels.

V. Study ZnO NW-FETs with different channel lengths (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m) and investigate the impact of the channel length ($L_{ch}$) scaling on electrical and optical characteristics. Furthermore, we describe a fabrication process of ZnO NW-FETs using a top-down fabrication starts with a thin-film deposition by remote plasma enhanced atomic layer deposition (PEALD). The remote PEALD is followed by aniso-tropically reactive ion etch (RIE) to produce ZnO NWs with different channel lengths (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m).

## 1.3 Thesis Outline

The thesis outline is as follow:

**Chapter 1:** The chapter introduces a general introduction of metal-semiconductor contacts, aims and objectives of PhD thesis, outlines an overview of the main points, and clarifies the structure of this thesis.

**Chapter 2:** This chapter gives an extensive theoretical background and a fundamental study of metal-semiconductor contact by looking at nanoscale properties of the interface between a metal and a semiconductor. The chapter also reported a transport properties and the formation of metal-semiconductor contacts. In addition, we also studied the impact of a metal work function on the metal-semiconductor interface as well, as a concept of Schottky barrier height has been discussed within a metal contact models: Schottky contact and Ohmic contact. In addition, we studied the basic fundamentals of transistor operation as well as a transmission line method (TLM). The chapter also studied the properties of ZnO including the crystal structure, physical properties, electronics and transmission properties and finally a brief introduction of methods used to syntheses zinc oxide.

**Chapter 3:** This chapter concludes the discussion of methodology and charac-

terisation techniques, as well as a chemical vapour deposition (CVD) process and set-up (basic fundamentals) and characterisation techniques used in thesis such as X-ray photo-electron spectroscopy (XPS), energy dispersive X-ray (ESM), photo luminescences (PL), their working principles used to analyse morphology and chemical characterization of ZnO NWs will be discussed as well. In addition, a technical details of four point probes measurement used to investigate the electrical characteristics will be introduced.

**Chapter 4:** This chapter presents a multi-scale simulation study of a nano-scale contact combining density functional theory (DFT) calculations with solutions of 1D Schrödinger-Poisson equation in order to understand a relation among contact resistance and band structure at the interface relevant to the future of sub-10 nm technology. The multi-scale simulations investigate a nano-scale contact made of a Ni metal interfacing an 11.0 nm thick InAs layer on a $p$-type doped $AlAs_{0.47}Sb_{0.53}$ buffer. A thermal reaction between Ni and InAs results in the formation of an 8.5 nm thick $Ni_3InAs$ layer leaving only a 2.5 nm thick of InAs acting as a channel which is treated as a heavily doped InAs layer. The DFT calculations reveal a band-gap narrowing in the InAs at the metal-semiconductors interface which substantially affects carrier transport through the Schottky barrier. The results given an exceptionally good agreement with experimental observation of metal contact sheet resistance.

**Chapter 5:** This chapter briefly studies and described a top-down fabrication method used to fabricate the ZnO TFTs with different channels (2 $\mu$m, 4 $\mu$m, 5 $\mu$m, and 10 $\mu$m) on a thermally oxidized Si substrate via PEALD. In addition, electrical characterisations have been carried out to study the impact of a scaling of channel length ($L_{\mathrm{ch}}$). The chapter also investigates the behaviour of a breakdown voltage and a sub-threshold current in ZnO TFTs with various channel lengths. A transmission line method (TLM) has been used to obtain contact resistance ($R_{\mathrm{C}}$), We obtained the effective ($\mu_{\mathrm{eff}}$) and channel ($\mu_{\mathrm{ch}}$) electron mobility for different channel length (2 $\mu$m, 4 $\mu$m, 5 $\mu$m, and 10 $\mu$m). The electron mobility is obtained from the expression for the drain current of MOSFET in a linear regime using a MOSFET basic theory. In addition, this chapter also overview the fabrication process of ZnO NW-FETs using a top-down fabrication. The top-down method fabricated ZnO NW-FETs which have three different channel lengths of (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m) are also overviewed in this chapter. The optical and electrical characterisations are carried out to study the effect of scaling a channel length ($L_{\mathrm{ch}}$) and investigates

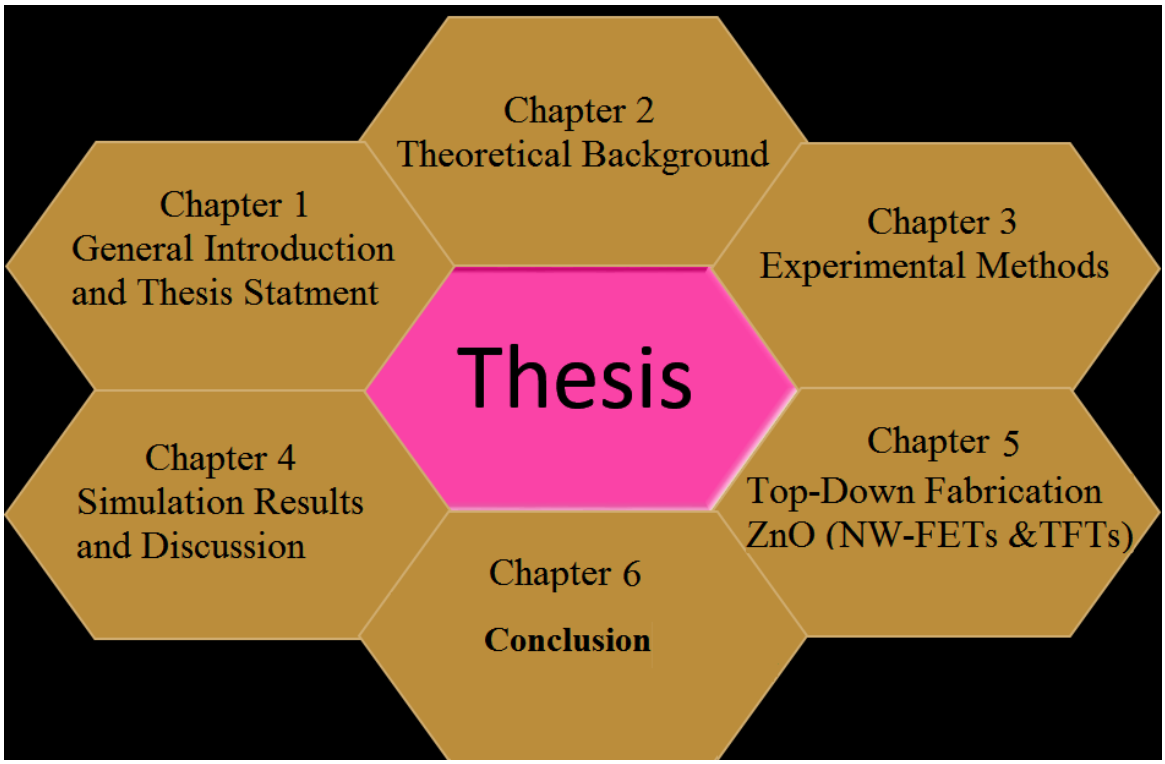


Figure 1.1: Schematic illustrating the layout of chapters in this thesis.

the sub-threshold current in ZnO NW-FETs with various channel lengths (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m).

**Chapter 6:** A conclusion of the thesis is summarized in this chapter. The chapter also provides an outlook and perspectives on future work directions for semiconductor devices made of ZnO as well as deeper understanding of nanoscale metal-semiconductors contacts. The layout of this thesis can be summarized in Fig. 1.1.

# References


[1] S. Adachi. *Properties of semiconductor alloys: group-IV, III-V and II-VI semiconductors*. Vol. 28. John Wiley and Sons, 2009 (cit. on p. 1).

[2] M. S. Simon and K. N. Kwok. *Physics of semiconductor devices*. John Wiley and Sons, 2006 (cit. on p. 1).

[3] *International technology Roadmap for semiconductors*. http://public.itrs.net. Accessed: 2015-06-30 (cit. on p. 1).

[4] S. M. Sultan, K. Sun, O. Clark, T. B. Masaud, Q. Fang, R. Gunn, J. Partridge, M. Allen, P. Ashburn, and H. M. H. Chong. "Electrical characteristics of top-down ZnO nanowire transistors using remote plasma ALD". In: *Electron Device Letters* 33.2 (2012), pp. 203–205 (cit. on p. 1).

[5] H. Liu. *Intersubband Transitions in Quantum Wells: Physics and Device Applications*. 1999 (cit. on p. 1).

[6] Z. Ye and M. Wong. "Characteristics of thin-film transistors fabricated on fluorinated zinc oxide". In: *Electron Device Letters* 33.4 (2012), pp. 549–551 (cit. on p. 2).

[7] S. Chu, G. Wang, W. Zhou, Y. Lin, L. Chernyak, J. Zhao, J. Kong, L. Li, J. Ren, and J. Liu. "Electrically Pumped Waveguide Lasing from ZnO Nanowires". In: *Nature Nanotechnology* 33.6 (2011), pp. 506–510 (cit. on p. 2).

[8] Ü. Özgür, Y. I. Alivov, C. Liu, A. Teke, M. Reshchikov, S. Doğan, V. Avrutin, S. J. Cho, and H. Morkoc. "A comprehensive review of ZnO materials and devices". In: *Journal of Applied Physics* 98.4 (2005), p. 11 (cit. on p. 2).

[9] S. M. Sze and K. K. Ng. *Physics of semiconductor devices*. John Wiley and Sons, 2006 (cit. on p. 2).

[10] H. Woong, P. Jong Bae, Y. Jongwon, K. Bong-Joong, S. Jung-Inn, L. Young-Boo, B. Tae-Sung, C. Sung-Jin, H. Yun-Suk, S. Byoungchul, A. S. Eric, L. Takhee, and E. W. Mark. "Tunable Electronic Transport Characteristics of Surface Architecture Controlled ZnO Nanowire Field Effect Transistors". In: *Nano Letters* 8.3 (2008), pp. 950–956 (cit. on p. 2).

[11] S. Kwon, S. Bang, S. Lee, S. Jeon, W. Jeong, H. Kim, S. C. Gong, H. J. Chang, H. Park, and H. Jeon. "Characteristics of the ZnO thin film transistor by atomic layer deposition at various temperatures". In: *Semiconductor Science and Technology* 24.3 (2009), p. 035015 (cit. on p. 2).

# Chapter 2

# Theoretical Background

## 2.1 Introduction

Every electronic device needs the interface supplies external forces aiming to impose a control over device operations. In practice, this interface will be between two or more materials (semiconductors, metals and insulators) [1]. Forming an ideal interface in electronic devices made of semiconductors has many challenges especially when devices have nano-scale dimensions. We can distinguish between the two types of metal-semiconductors contacts according their functionality as a metal-semiconductor junction in rectifying the current:

1. Rectifying junction called Schottky contact [2].

2. Non-rectifying junction called Ohmic contact [3].

Fig. 2.1(a, b) shows a schematic energy diagram of metal-semiconductor interface. The difference in energy between Fermi energy and vacuum level is defined as a work function ($\phi_M$) [2]. This value corresponds to the minimum amount of energy needed to remove an electron from a metal, which is use to align the metal and the semiconductor together [4]. Fig. 2.1(b) also shows that, electron affinity $\chi$ is defined as the energy needed to move electrons from vacuum level to conduction band as follows:

$$\chi = E_0 - E_F \tag{2.1}$$

where $\chi$ is the electron affinity, $E_0$ is the vacuum level, $E_F$ is a Fermi level. Furthermore, the schematic shows the energy diagram of a $p$-type semiconductor, where

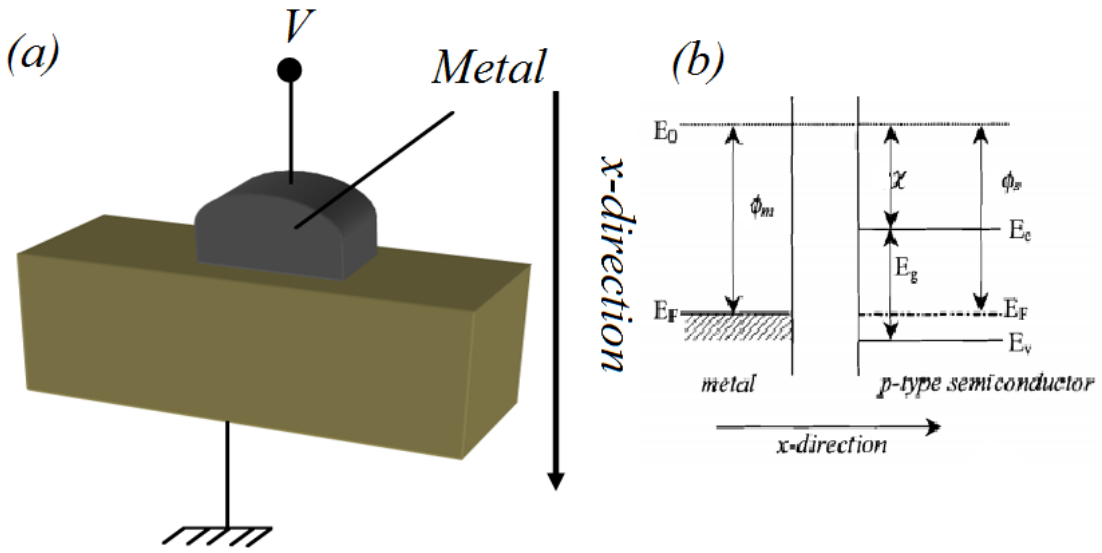


Figure 2.1: (a) Perspective view of metal semiconductor contact, (b) energy band gap diagram of metal-semiconductor junction, where $\Phi_M$ is the metal work function, $\phi_S$ is the Schottky barrier height, $E_F$ is the Fermi level, $\chi$ is the electron affinity, $E_C$, $E_V$ are the conduction and valence bands, respectively.

$E_V$ is the valence band and $E_C$ is the conduction band separated by a band gap ($E_G$). If Fermi levels of a metal and a semiconductor are aligned, an ideal metal-semiconductor contact can be formed [1]. If there is no movement for the electrons during the process, the band diagram for the contact can be described as shown in Fig. 2.1(b). Therefore, an ideal metal-semiconductor contact can be defined by these assumptions:

1. The metal and the semiconductor are well contacted. There is no oxide or charge layers between the metal and the semiconductor [3].

2. No impurities are at interface between the metal and the semiconductor [5].

This chapter examines the basic theory of metal-semiconductor contacts. In addition, we will illustrate the ideal and real energy band diagrams of a metal-semiconductor interface which determine the conduction properties of the metal-semiconductor contacts for the current transport processes mechanism. We will also undergo through basic principles of transistors including threshold voltage, scaling theory, short channel effects, drain induce barrier lowering and back gate transistor design. Furthermore, the transmission line method used for calculation of channel mobility will be discussed. Finally, a comprehensive introduction about ZnO synthesis, properties and structure will be presented.

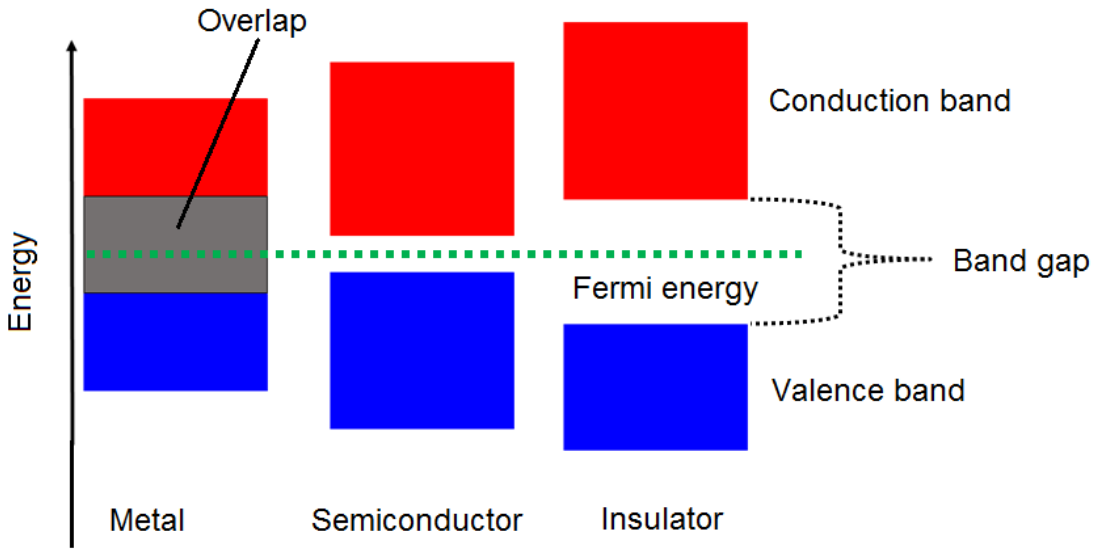


Figure 2.2: Electronic band structures of metals, semiconductors and insulators.

## 2.2 Energy Band Structure

The band gap energy of material refers to the difference between the top of the valence band and the bottom of the conduction band in a material [2]. If a substance has a large band gap, the material is called insulators. A substance with a smaller band gaps are generally called semiconductors, while the conductors have very small band gaps or the band gap is zero due to the overlap in valence and conduction bands as it shows in Fig. 2.2 [2]. In addition, the band gap structure is responsible for the electrical characteristics. For instance, in the semiconductors and the insulators, the electrons confine to energy bands and are banned from other regions [6]. If an electron is able to jump from a band to another, a minimum energy is required for the transition. An electron can gain the require energy to jump to the conduction band by absorbing either a phonon (heat) or a photon (light) [2]. If the conduction band minimum and the valence band maximum are at the same k-wave-vector point in the band-structure, the energy band gap is called a direct band gap. If the conduction band minimum and the valence band maximum are not at the same **k**-wave-vector, the energy band gap is called a indirect band gap [7]. For example, the indirect band gap semiconductors are germanium and silicon, and the direct band gap are gallium arsenide [7]. This can provide more efficient absorption and emission light for semiconductors device [8].

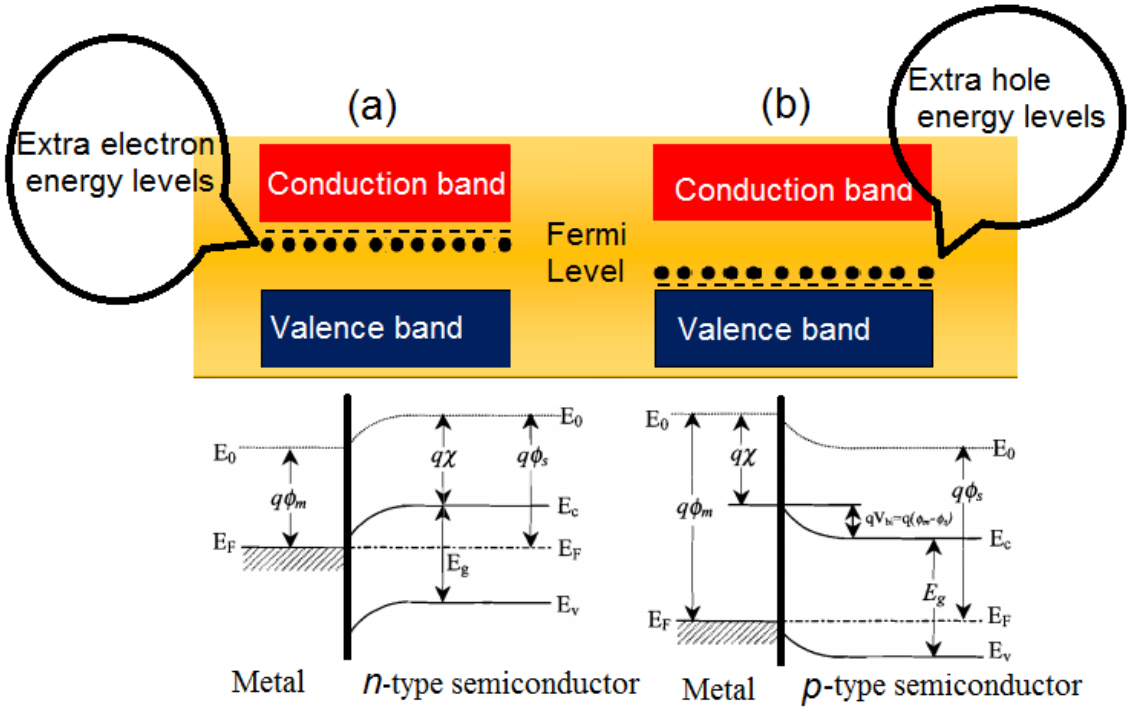


Figure 2.3: (a) $n$-type metal-semiconductor band gap diagram, (b) $p$-type metal-semiconductor band gap diagram.

## 2.3 Band Gaps For The Doped Semiconductors

There are two types of doping in semiconductors: $n$-type and $p$-type [9]. For the $n$-type semiconductors, the electron energy level is close to the top of the band gap. Therefore, it is easy for an electron to be excited into the conduction band [3] because the added donor impurities contribute to the electron energy levels in the band gap. Therefore, the electron excited into the conduction band shifts Fermi level about half way between the donor level and the conduction band [10]. In other words, the electron elevated to the conduction band with an energy applied by external electric field moves through the material as shown in Fig. 2.3(a). The $p$-type semiconductors have added acceptor which contributes to the hole energy level. Therefore, an electron can be excited from the valence band into these levels which leaves a mobile hole in the valence band. Notice that the shift in Fermi level about half way between the acceptor level and the valence band as shown in Fig. 2.3(b).

## 2.4 Metal Work Function

Metal work function is defined as a minimum energy needed to move an electron from a metal [4]. Fig. 2.4(a) shows the schematic energy diagram of different metal work functions. The valence band is occupied with the electrons up to the Fermi energy level [2]. The difference in energy between Fermi energy and vacuum level is thus defined as the work function ($\phi_M$) as shown in the following equation:

$$\phi_M = E_0 - E_F \tag{2.2}$$

And the work function ($\phi_M$) for a given surface can be expressed as:

$$\phi_M = -qW - E_F \tag{2.3}$$

where ($-q$) is the charge of an electron, $W$ is the electrostatic potential in the vacuum near the surface, and $E_F$ is the Fermi level, while $\phi_M$ refers to the metal work function. The term $-q\ \phi$ is the energy of an electron at rest in the vacuum nearby the surface as shown in Fig. 2.4(b). The figure shows the work function for some metal. The values have been taken from Ref. [4].

## 2.5 Schottky Barrier Height

Schottky barrier height (SBH) is defined as the difference between Fermi level and the band edge [4]. This potential barrier forms when the Fermi energy of the metal and the semiconductor are aligned together as it shows in Fig. 2.5. Since the Schottky barriers leads to rectifying behaviour of a contact, the barrier can be used as a diode which acts as a single metal-semiconductor junction with a rectifying behaviour. Schottky barrier height behaves differently for $p$-type and $n$-type semiconductors. The alignment of semiconductor ($p$-type or $n$-type semiconductor) bands near the junction is independent to the doping level [4]. The mechanism to extract Schottky barrier height has been addressed by different groups [4]. One of the most effective method to extract Schottky barrier height is to assume that, the barrier is proportional to the difference between the metal work function and the semiconductor electron affinity [4] as shown in Eqs. (2.4) and (2.5). Let us consider that, a metal and a semiconductor are brought together at thermal equilibrium, and Fermi

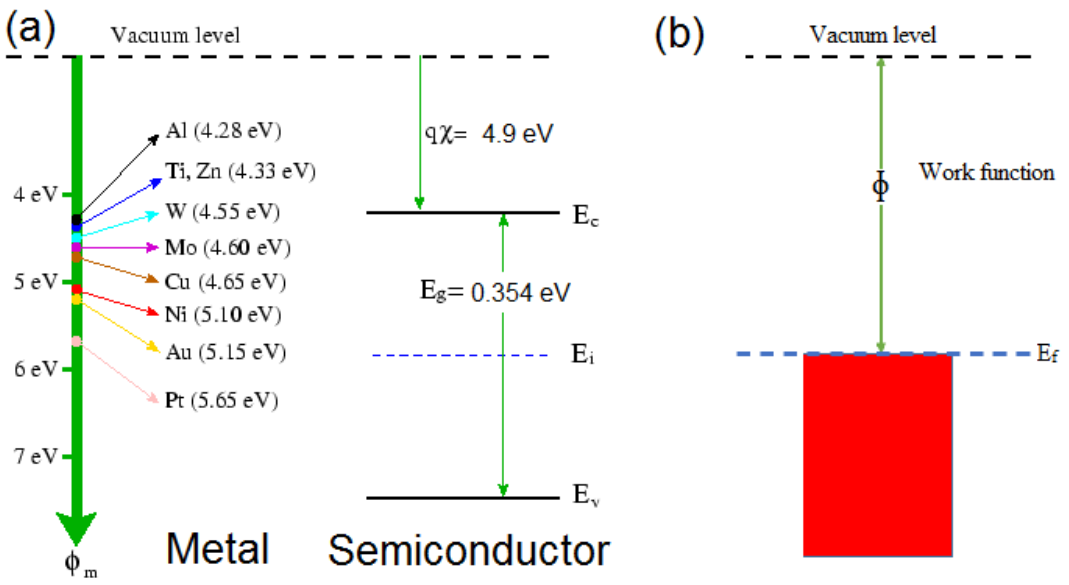


Figure 2.4: (a) Band gap diagram of InAs semiconductors and metal work function for some material. (b) Schematic shows the metal work function definition.

energy of these two materials is equal as shown in Fig. 2.5. Then Schottky barrier height for the $n$-type semiconductors can be written as:

$$\phi_{Bn} = \phi_M - \chi_S \tag{2.4}$$

where $\phi_{Bn}$ is the Schottky barrier for electrons, $\phi_M$ is the metal work function, $\phi_S$ is the semiconductor work function and $\chi$ is the affinity. Schottky barrier height for holes, $\phi_{Bp}$, is defined as:

$$\phi_{Bp} = E_G + \chi_S - \phi_M \tag{2.5}$$

were $E_G$ is the energy band gap and q is the electron charge.

## 2.6 Ohmic Contact

An Ohmic contact is a non-rectifying contact junction that occurs between two conductors. If the junction is formed between a metal and a semiconductor, the junction allows the current to flow both ways (equally) within a normal operation

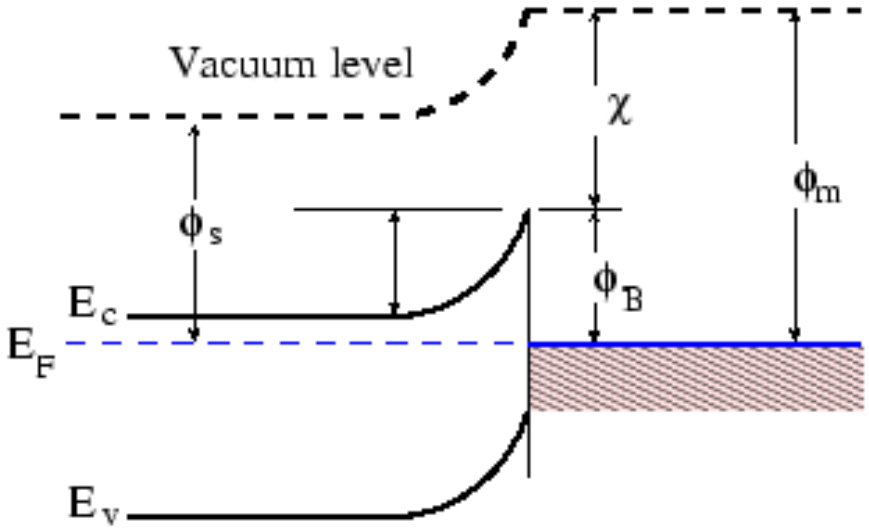


Figure 2.5: Band gap structure of metal-semiconductor contact at thermal equilibrium.

range junction as shown in Fig. 2.6(b) [11]. Fig. 2.6(a) shows that Ohmic contact has a voltage-current characteristic ($I-V$ characteristic) close to resistor, the junction between the two conductors have a linear current-voltage curve (Ohm law) [11]. For the Ohmic contact, Schottky barrier height is not pronounced (zero or negative values) [9].

## 2.7 Current Transport Mechanisms

To study the current transport across the interface between a metal and a semiconductor, it is well worth to address the carrier transport mechanism through the contact [6]. Transport at the interface between metal and semiconductor occurs in three ways:

1. Electrons transport from the metal over the potential barrier into the semiconductor [12]. This type of transport can be categorised into: thermionic emission and diffusion, these three types are the dominant processes for lightly doped material operating at room temperature [13].

2. Quantum-mechanical tunnelling of electrons through the potential barrier for a heavily doped semiconductor operating at low temperature [14]. When the

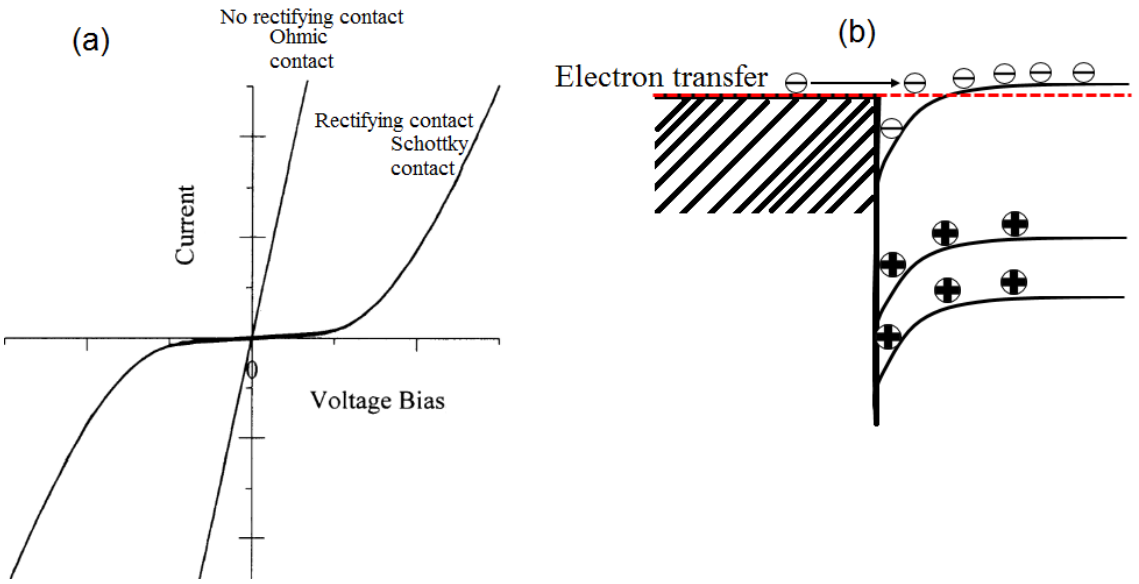


Figure 2.6: Current-voltage characteristics of (a) an Ohmic contact and Schottky contact of a metal-semiconductor interface, (b) the energy alignments of the metal contacting with a semiconductor in the case of the Ohmic contact.

thermal energy of a carrier is not enough to reach the top of the barrier, the electron has a probability to penetrate through the barrier. When temperature increases, the electron becomes more excited and gain more energy. This energy increases the tunnelling probability and the potential barrier becomes lower [6]. If the semiconductors are heavily doped, the depletion region becomes smaller, as a result, the probability of tunnelling will increase which leads to obtain an Ohmic contact [2]. This heavily doped layer can be formed by ion implantation or by direct doping as shown in Fig. 2.7.

3. Charge carrier generation in the space charge region. This process is due to the presence of generation-recombination centres in the band gap region [7].

4. Recombination of electrons and holes in the neutral region (hole injection) [7].

## 2.8 MOSFET Physics

Metal-oxide semiconductor field effect transistors (MOSFETs) consist of three terminals device where current between two terminals can be controlled by applied voltage through the third terminal [15]. The three terminals are normally called (source, drain, and gate) as it shows in Fig. 2.8(a) [15]. Transistors are normally used for two operations: switching and amplification. Switching operation is move

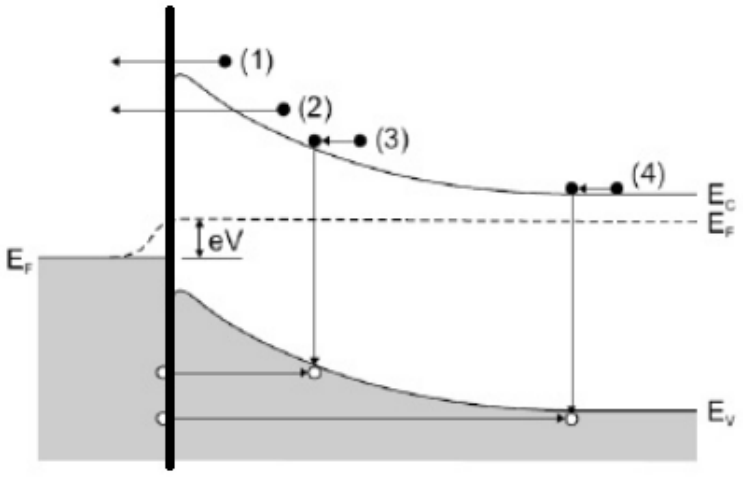


Figure 2.7: Transport mechanisms at metal-semiconductor junctions.

of a transistor between the two states: the off-current (a blocked state) and the on-current (a current passing). Amplification can be achieved by applying a small current (AC) signal to the third terminal in order to generate a larger signal between the other two terminals [16]. A transistor consists an active channel through which charge carriers, electrons or holes, flow from a source to a drain [17]. Therefore, a channel length ($L_{ch}$) can be defined by the distance between the source and the drain [18]. The source and drain terminals are connected to the semiconductor through Ohmic contacts. The conductivity of the channel is a function of the potential applied across the source and drain terminals. Transistor operation can be characterised by device parameters such as a threshold voltage $V_{Th}$, a sub-threshold slope (SS), a maximum on-current, and gate and drain transconductance. The thin oxide layer acts as an isolator to isolate the channel region from the gate. The gate is usually on the top of the channel to effectively control a carrier flow in the channel but the gate can be also at the bottom of the device body (a back gate) as we will discuss later in this chapter. Transistors have two modes of operational regimes: a linear regime and a saturation regime as shown in Fig 2.8(b). If there is no current flow between drain and source (at zero gate voltage), the device is normally off (enhancement mode device). On the other hand, if the current flow from the drain to the source, the device is normally on (depletion mode device) [17].

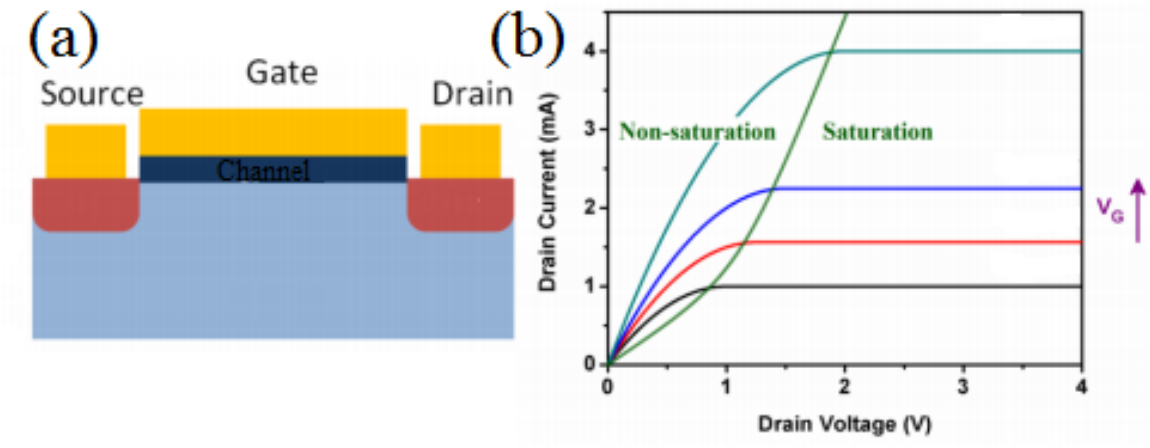


Figure 2.8: (a) Cross section of $n$-channel MOSFET structure. (b) Transistor operation modes of a typical $n$-channel enhancement mode MOSFET.

### 2.8.1 Scaling Theory

Scaling theory is an approach enables billions of transistors to be placed on a single chip in order to achieve a high performance and high density transistors. The increasement in scaling demand brought the benefit of cost reduction, increase in device performance, increase in switching speed, and low cost of manufacturing for semiconductor industries [19]. Scaling of device dimensions has to follow requirements of the International Technology Roadmap for Semiconductors (ITRS). The ITRS has comprehensive documents widely used as a guide and a reference that enables the semiconductor industries to transform the scaling rules into reality for semiconductor device research and manufacturing [9].

The ITRS has three contributions. The first contribution is to identify the requirements that can be met by technology solutions currently under the development. The second contribution is to recognize the existence of interim solutions for the medium term challenges, problems and their limitations at the present time. Finally, the third contribution is to identify the areas where there are no known manufacturing solutions customarily labelled as the red brick wall to induce the industry to concentrate on them strategically and focus research efforts in these areas [19].

The edition of ITRS-2003 has set the main objectives and targets to 2018. This version is based on research from the semiconductor industries and ITRS outlines the requirements and identifies the challenges over the next 15 years. Fig. 2.9 demonstrates the trend in MOSFETs channel length scaling [20].

Scaling scheme for MOSFETs can be considered for the following parameters: the

Table 2.1: Classical MOSFETs scaling parameters versus the scaling factor of each parameter.

| Device Parameter | Scaling factor |
|---|---|
| Length | $1/K$ |
| Width | $1/K$ |
| Oxide Sickness | $1/K$ |
| Voltage | $1/K$ |
| Capacitance | $1/K$ |
| Doping concentration | $K$ |

total device length ($L_{SD}$), gate length ($L_G$), oxide thickness, doping concentration and the gate voltage. The horizontal dimensions ($L_{SD}$) and ($L_G$) are the most interesting parameters for the study of electron transport. The scaling of transistor dimensions and device parameters can be achieved by considering a scale factor for each dimension and parameter. Table 2.1 shows the classical MOSFET scaling parameters versus the scaling factor ($K$) of each dimension or parameter.

In addition, the reduction in area between the source to the drain (channel region) of a MOSFET leads to an effect which known as a short channel effect. one of the most undesirable short-channel effect is a threshold voltage at which the device turns on, especially at high drain voltages as we will discuss it into a more details in the next section [19].

### 2.8.2 Short Channel Effects

As the distance between the source and drain reduces, the channel length of MOSFET becomes shorter which leads to so-called short-channel effects [21]. For example, if the drain voltage is applied, the potential barrier along the channel decreases. Therefore, the electrons are more free to move between the source and drain. However, the space charge at the drain interacts with the moving electrons, which leads to further decrease in the potential barrier at the source to the channel region [17]. The reduction of the potential barrier allows the electrons to increase a flow between the source and the drain and eventually leads to the effect of a drain-induced

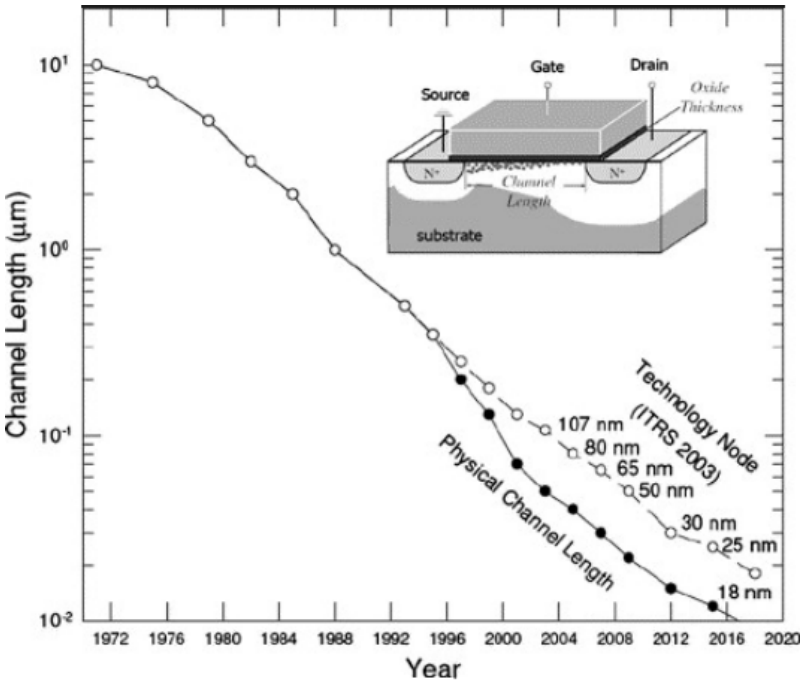


Figure 2.9: The trend in MOS channel length scaling and the prediction made in the 2003 International Technology Roadmap for Semiconductors [9].

barrier lowering (DIBL) [22]. The reduction in channel length leads to increase in electron velocity as well as the increase in electron density which leads to increase in a maximum drain current [21]. Short-channel effects can be attributed into:

i. the limitation imposed on electron drift characteristics in the channel region. In this case, the drift transport of the electrons are confined in the channel region. The effects can clearly be seen in the mobility degradation and carrier velocity saturation [17].

ii. A modification of the threshold voltage due to shortening channel length as a channel length decreases. the threshold voltage decreases. Since the source to the drain region decreases the charge depleted in the source-drain region, hence the threshold voltage becomes more pronounced [23].

iii. Drain induced barrier lowering (DIBL). If the drain voltage is increased in a short channel transistor. The potential barrier normally stops the electrons from flowing from the source to the drain. By reducing the channel length, and applying a gate voltage, this affects the potential barrier. Therefore, the electrons are able to flow between and through the barrier. More details will be explained in the next section.

iv. Punch through channel length modulation in a MOSFET. The effect is caused by the increase in the depletion layer width at the drain region. As the drain voltage is increased, the channel length reduces because the potential barrier is lowered. Eventually, the potential barrier is so small that electron will flow between the source and the drain even if the gate bias is smaller than the threshold voltage. This effect is called punch-through. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device [22].

v. Surface scattering, the effect is defined as the collisions suffered by the electrons that are accelerated toward the interface. When the carriers travel along the channel, they are attracted to the surface by the electric field created by the gate voltage. As a result, the carriers will interact with the surface potential during their travel along the channel. Since the carrier transport is confined within the narrowed inversion layer, this effectively reduces the surface mobility of the carriers [17].

vi. Velocity saturation. This effect occurs when the carrier velocity begin to reduce as the electric field increases. In other words, when the electric field increases, carrier velocity tends to saturate and carriers eventually cannot move faster. Velocity saturation is caused by the increased scattering rate for highly energetic carriers [23].

vii. Impact ionization. The impact ionization occurs when the energetic charge carrier loses energy by creating other charge carriers. In other words, the carriers have a high enough energy to cause an effect which is called hot carriers. These normally appears close to the drain, where they have the largest kinetic energy [21].

viii. Hot electrons or hot carrier effects. These effects occur when high electric field causes hot carriers to hit the atoms near the drain at a high speed and create an ionisation impact, which causes a substrate and gate currents [21].

### 2.8.3 Threshold Voltage and Sub-Threshold Current

Threshold voltage $V_{Th}$ a fundamental parameter in circuit design and testing, as well as in technology characterization of MOSFET [23]. The threshold voltage can be defined as the minimum gate-to-source voltage ($V_G$) that is needed to create a conducting path between the source and drain [23]. Generally, the gate voltage at which the device starts to turn on defines as a threshold voltage. The accurate value of threshold voltage is important to associate a correct behaviour of MOSFET. Many methods can be used to extract threshold voltage, the majority of these methods are based on the inversion operation characteristics [17]. The most common methods can be listed as follows:

i. Defining $V_{Th}$ as the gate voltage corresponding to a certain predefined practical constant drain current.

ii. Defining $V_{Th}$ by finding a gate voltage axis intercept of a linear extrapolation of $I_D$–$V_G$ characteristics at its maximum first derivative (slope) point with a zero drain current.

iii. Determining $V_{Th}$ at the maximum of the second derivative of $I_D$ with respect to $V_G$ [23].

When the gate bias is less than the threshold voltage ($V_G$<$V_{Th}$), an undesirable leakage current can be occurred at the drain contact. In this case, the MOSFET current observed at $V_G$<$V_{Th}$ is called the sub-threshold current or the off-state current, $I_{off}$ [24]. The sub-threshold drain current is typically very small in well design MOSFETs. The accessement of sub-threshold slope, when the drain current is plotted on a logarithmic scale as a function of the gate bias at a fixed drain bias [24].

### 2.8.4 Drain Induced Barrier Lowering

Drain induced barrier lowering (DIBL) is a short-channel effect in a MOSFET which refers to a reduction of threshold voltage for a transistor at high drain voltages [22]. When the channel length becomes shorter, the increase in potential from the drain can penetrate toward the source, and along the channel, this can lower the barrier at the channel region which leads open the channel even at small applied gate bias [21].

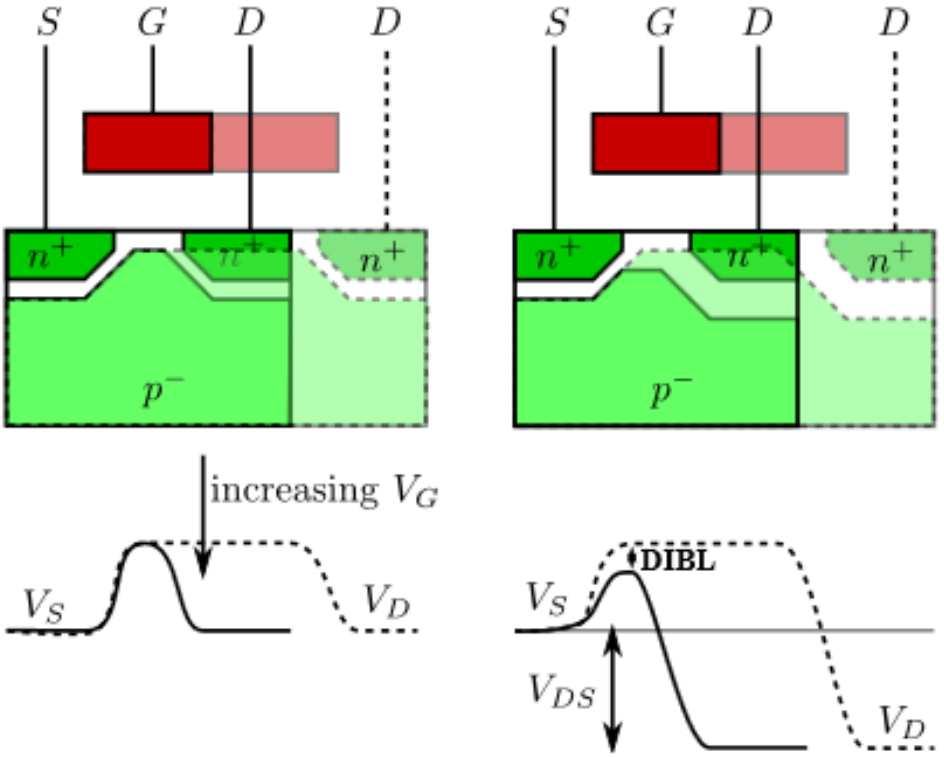


Figure 2.10: The top schematics show a cut of long-channel (dashed line) and short channel (solid line) MOSFETs. The bottom schematics show the change in potential barrier profile along the surface of the channel (from the source to the drain). The dash line shows the potential barrier along the channel in a long-channel MOSFET while the solid line show the movement/decrease of the potential barrier along the channel in a short-channel MOSFET. On the left side, $V_D$=0, while on the right side, the drain voltage is large to show the DIBL effect [22].

In other words, as the voltage between the source and drain increases, the depletion region under the drain can lower the potential barrier of the source-to-channel junction. If the barrier between the source and channel is decreased, electrons are more free to inject into the channel region as it shows in Fig. 2.10. In this case, threshold voltage is lowered, and the gate has less control of the channel [22].

### 2.8.5 Back Gate in Transistor

Back gate is a relatively convenient way to control carrier transport in a large transistor because it can be fabricated as a large area metal contact on the bottom of the device. The back gate can be fabricates directly under the device by etching off the substrate [25]. To understand the back gate functioning, Fig. 2.11 shows a Si back gate in a FET. When a back gate bias $V_{BG}$ is applied, a current path will be

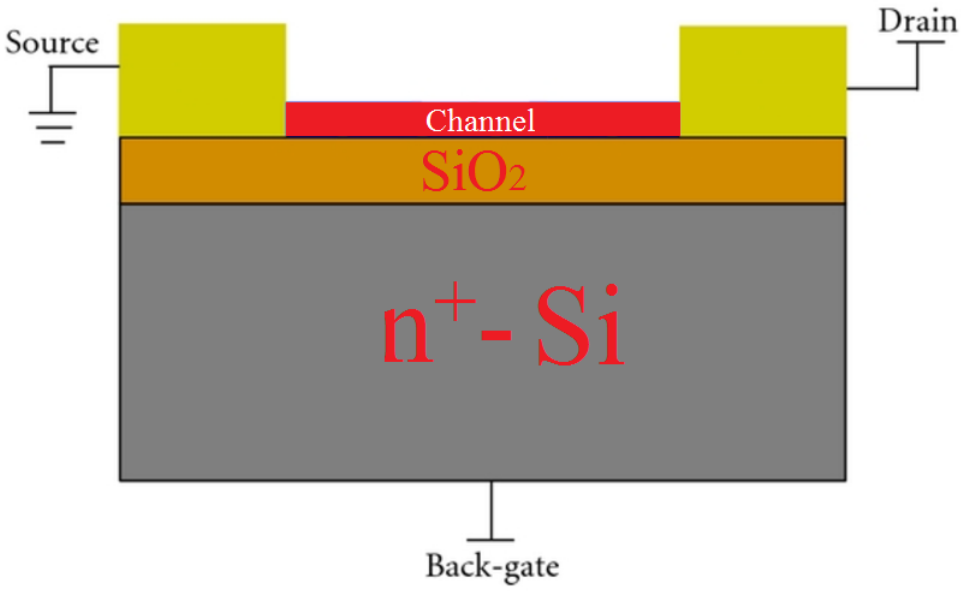


Figure 2.11: Schematic illustrates $n$ type Si-FET backed gate.

formed at the back side of device. This allows electrons to flow along the channel from the source to the drain [26]. We can make this conductive channel wider or smaller by applying a suitable gate potential [25].

From a device design point of view, the most important consideration for the back gate design is a metal work function. This is use of the back gate to open the opportunity of choosing an appropriate work function of the gate and redesign the device to achieve the best combination of work function and channel doping. In order for the back gate to deplete the channel, appropriate metal with a suitable work function can be used in the way than a possitive gate bias $V_{BG}$ has to be applied to open the channel. The positive charge on the gate pushes the mobile holes into the substrate. Therefore, the gate is depleted the mobile carriers at the interface and a negative charge, due to the ionized acceptor ions is left in the space charge region. Then the transistor will be operating as normally-on device.

## 2.9 Transmission Line Method

Transmission line method (TLM) is a technique used to assess the electrical properties as well as Ohmic contacts of electronic devices [27]. TLM was proposed by Reeves and Harrison [27]. This section explains how a TLM can be used to extract the contact resistance of a transistor. Fig. 2.12 shows a schematic diagram of the

TLM structure. The structure consists of a rectangular metal contact with different spaces between contacts ($L$) and $W$ is the width of the rectangular metal contact. To apply the TLM, the four point probes, where a constant current is supplied by three probes. The total resistance ($R_{Tot}$) between two neighbouring contact pads and separated by a distance ($L$) can be written as follow:

$$R_{Tot} = \frac{2R_{sk}L_T}{W} + \frac{R_{sh}L}{W} \tag{2.6}$$

where $R_{sh}$ and $R_{sk}$ are the semiconductor sheet resistance between the contact pads and under the contact pads respectively, $L_T$ is the transfer length and refers to the distance across which most of the current transfers into the contact pads from the semiconductor [10]. Notice that a plot of $R_{Tot}$ vs. length ($L_T$) can obtain a contact resistance by extrapolation to the horizontal ($x$) axis at $L = 0$. Therefore, in the limit of a zero-length ($L = 0$), the residual resistance is twice as much the contact resistance ($2R_C$). The intercept = $2L_T$ as shown in Fig. 2.13 is an example of plot a total resistance as a function of TLM pad spaces [10]. We can write the following equation:

$$R_{Tot} = 2R_C + \frac{R_{sh}L}{W} \tag{2.7}$$

If the voltage dropped in the horizontal direction is attributed to the current flow in semiconductor sheet resistance ($R_{sh}$), while the voltage dropped in the vertical direction, perpendicular to the plane of the current, therefore, the total resistance can be function in all direction and both length and width, the Eq. (2.7) can be written as the following:

$$R_{\mathrm{Tot}} = \frac{2R_CL}{W} + \frac{R_{Sh}L}{W} \tag{2.8}$$

In addition, the slope of the line in Fig. 2.13 gives the value of $R_{sh}$/W and the intercept with $y$-axis gives the value of $2R_C$. Notice that, the intercept with $x$-axis is called $L_x$ and it is related to the transfer length $L_T$ as follow:

$$L_x = \frac{2R_CW}{R_{sk}} = 2L_T \tag{2.9}$$

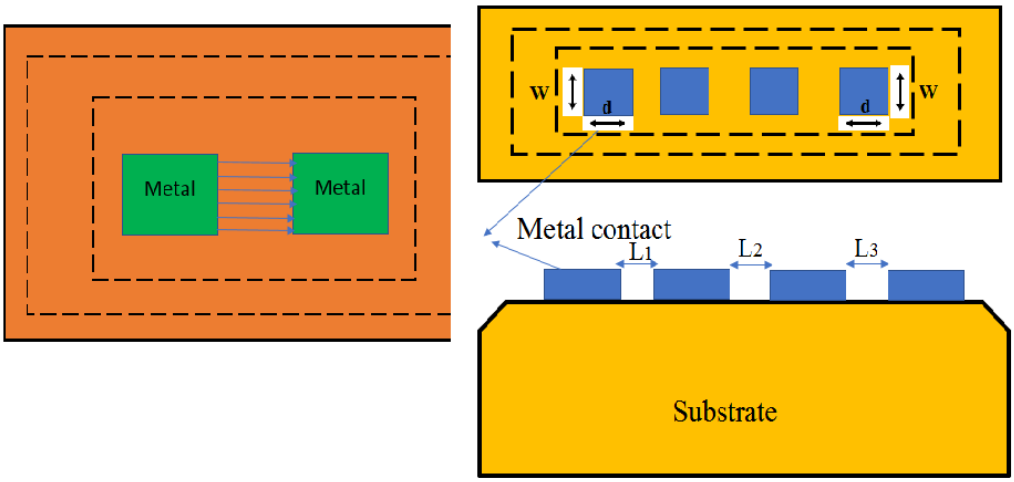


Figure 2.12: Schematic diagram shows the TLM structure.

If the contact pad length ($d$) is much larger than the transfer length $L_T$ ($d$>$L_T$), the effective contact area approximately takes the value ($W.L_T$) instead of ($W.d$). Thus, the specific contact resistance $\rho_C$ from the above equation becomes:

$$\rho_C = R_C\, W L_T = \frac{(R_C W)^2}{R_{sk}} \tag{2.10}$$

Eq. (2.10) is valid for the one-dimensional transmission line model (1D-TLM). This is based on the assumption that the current flows laterally from one contact to other contact [21]. Since the specific contact resistance can be measured, the contact resistance can be calculated using Eq. (2.10). The value of $R_C$ is independent of the contact length ($d$) and depends on the width and only on the dimension perpendicular to the current flow. In order to normalise the contact resistance, the value of $R_C$ is multiplied by the with ($W$) to obtain a value in $\Omega.\text{cm}^{-2}$ [10].

## 2.10 Effective Electron Mobility

Electron mobility ($\mu_{\text{eff}}$) is a quanity which measures how quickly an electron can move through a metal or semiconductor, when the electron is accelerated by an electric field. $\mu_{\text{eff}}$ can be also defined as a drift velocity per unit electric field [28]. Band structure of a semiconductor allows for two types of carriers: electrons and holes. A mobility of electrons can be very different from a mobility of holes because difference in semiconductor band structure and scattering mechanisms [28].

Effective electron mobility ($\mu_{\text{eff}}$) in MOSFETs is the mobility related to the total cur-

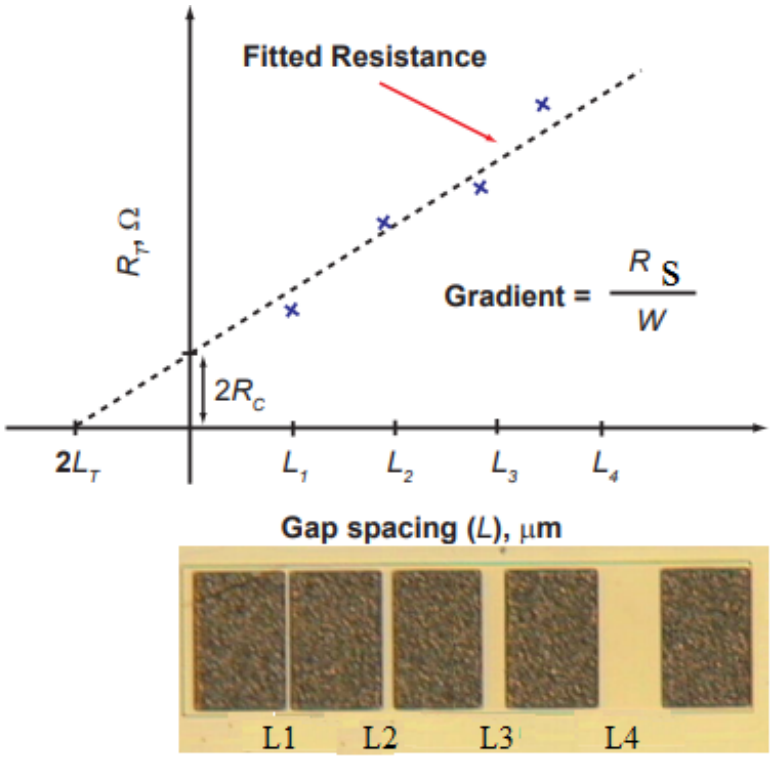


Figure 2.13: An example of a plot of total resistance as a function of TLM pad spacing.

rent measured in a device including any access resistance as shown in Eq. (2.11) [28]. $\mu_{\text{eff}}$ can be impacted not just by a channel conductance but also by access resistance and, eventually, also by external resistance of the source/drain contacts [29]. A general formula derived from a MOSFETs theory to calculate the mobility can be written as [28]:

$$\mu_{\text{n}} = \frac{I_D L}{C_{ox}[V_G - V_T]V_D} \tag{2.11}$$

We can use a linear approximation to calculate the electron effective mobility. To simplify Eq. (2.9), we can write the electron mobility $\mu_{\text{eff}}$ as:

$$\mu_{\text{eff}} = \frac{dI_{\text{D}}}{dV_{\text{G}}} \frac{L}{WC_{ox}V_{\text{D}}} \tag{2.12}$$

Therefore,

$$\mu_{\text{eff}} = M_{\text{lin}} \frac{L}{C_{ox}WV_D} \tag{2.13}$$

where is $M_{\text{lin}} = \frac{dI_{\text{D}}}{dV_{\text{G}}}$ is the slope and $\mu_{\text{eff}}$ is the effective electron mobility.

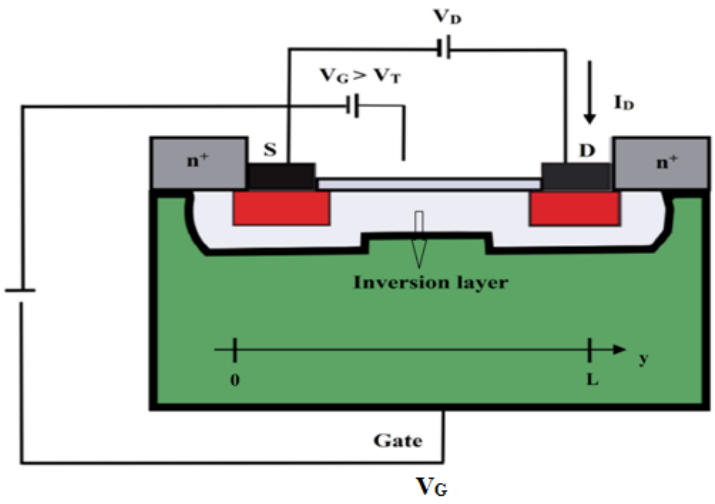


Figure 2.14: Schematic diagram of a field-effect transistor to extract the channel current and electron mobility.

## 2.11 ZnO Properties and Structure

Zinc oxide (ZnO) has a significant attraction as a semiconductor material for transparent high power electronics, solar cells, light-emitters, opto-electronics, gas sensors, and surface acoustic wave devices [18]. ZnO is known as a cheap and easily fabricated semiconductor which can be formed into various forms and morphological structures such as thin-film, NWs, nano-coating, nano-springs and nano-combs [30, 31]. Therefore, a great effort is dedicated to develop a fabrication method for a high quality of ZnO exhibiting excellent optical, electrical, and electronic characteristics [32]. A large number of various methods have been reported for ZnO synthesis based on bottom-up and top-down techniques [18, 30]. In the next section, the structure properties of ZnO will be discussed and physical parameters of ZnO will be overviewed.

### 2.11.1 ZnO Crystal Structural and Chemical Binding

ZnO structure belongs to a semiconductor compound which consists of two groups (group II for Zn and VI for O) [33]. Zinc element has five stabled isotopes. Common isotopes are $Zn^{64}$ (49.17 %), $Zn^{66}$ (27.73 %), $Zn^{67}$ 4.04 % and $Zn^{68}$ (18.45 %). Oxygen consists of a isotope O (99.76 %). Electron configuration of Zn is ($1s^2$), ($2s^2$), ($2p^6$), ($3s^2$), ($3p^6$), ($3d^{10}$) and ($4s^2$) while oxygen configuration is (1s), (2s) and (2p) [33]. ZnO has crystalline stable wurtize structure at room temperature [34].

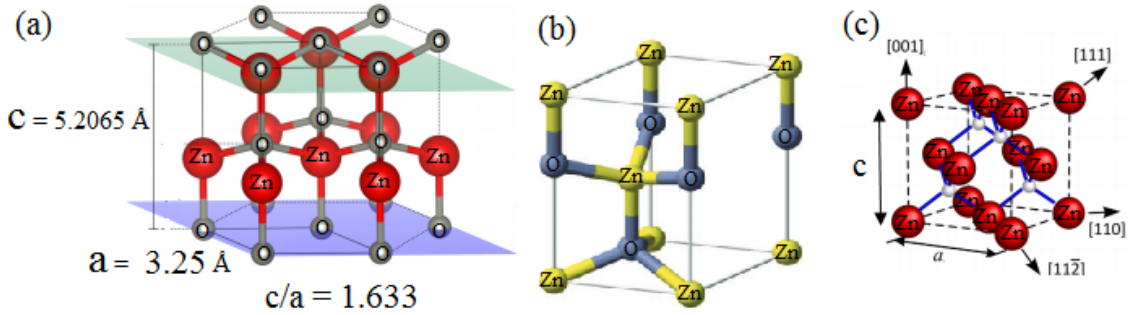


Figure 2.15: (a) ZnO wurtzite structure blue and green planes represent the rows of Zn and O charged planes. Red is reserved for O, Gray for Z [34]. (b) The wurtzite unit cell of a non-centre symmetric structure. (c) Various crystal planes of ZnO wurtzite structure show the hexagonal each anion of ZnO surrounded by four cations.

Fig. 2.15(a) illustrates the wurtzite structure of ZnO. The structure demonstrates a hexagonal unit cell with two lattice parameters ($a = 3.25$ $\mathring{A}$ and $c = 5.2065$ $\mathring{A}$). The ratio between them is $c/a = 1.633$. The hexagonal lattice belongs to a space group ($hcp$=$P63mc$) [31]. Fig. 2.15(b) demonstrates the wurtzite unit cell, the structure consists of two inter-penetrating hexagonal packed ($hcp$) sub-lattices. Each sub-lattice has one unit (Zn and O) combined together along the $c$-axis direction. The structure consists of two tetrahedral coordinates of $O^{2-}$ and $Zn^{2+}$ ions stacked along the $c$-axis [21]. Moreover, the tetrahedral structure in Fig. 2.15(b) shows a non-centre symmetric behaviour. Therefore, the centre of symmetry in the crystal structure displays inversion symmetry [34]. The wurtzite of ZnO has four common faces which are Zn-terminated (0001), O-terminated (000$\bar{1}$), $c$-axis oriented (2$\bar{1}$ $\bar{1}$0), and non-polar (01$\bar{1}$0) which consists an equal number of Zn and O atoms in the crystal structure [33]. The faces (0001) and (000$\bar{1}$) are categorised as a polar and play a role in ZnO applications. In the hexagonal ZnO, each anion is surrounded by four cations at the centre of each tetrahedral as shown in Fig. 2.15(c) [33]. Table 2.1 summarizes a data of ZnO crystal structures showing basic physical parameters of ZnO.

### 2.11.2 ZnO Physical Properties

ZnO is a wide band gap semiconductor (3.37 eV) at room temperature. ZnO has been reported as $n$-type semiconductor in nature due to the presence of native defects in their crystal structure such as oxygen vacancies and zinc interstitials [34]. The oxygen vacancies in ZnO are (+2). This demonstrates that the oxygen vacancies

Table 2.2: The basic physical parameters of ZnO.

| Parameter | Value |
|---|---|
| Stable Phase at 300K | Wurtzite |
| Lattice constant | a = 3.246 Å and c = 5.207 Å |
| Cohesive energy | 1.89 eV |
| Melting point | 1975° C |
| Thermal conductivity | 25 W/mK at 20° C |
| Band gap at RT | 3.37 eV (direct) |
| Electron effective mass | 0.24 $m_0$ |
| Hole effective mass | 0.59 $m_0$ |
| Debye temperature | 370° K |
| Lattice energy | 964 kcal/mole |
| Dielectric constant | 8.75 |
| Exciton binding energy | 60 meV |
| Piezoelectric coefficient | 12 pC/N |

are a dominant donor and thus are responsible for unintentional $n$-type conductivity as well as for a non-stoichiometry of ZnO. A mobility of electrons in ZnO has an estimated value between 1 to 100 $cm^2V/s$ at room temperature [31] which strongly depends on a material consistence. Electron and hole effective masses are estimated to be around 0.24 $m_0$ and 0.59 $m_0$, respectively, where $m_0$ is the electron mass in vacuum [31]. Table 2.2 shows the basic physical parameters of ZnO. ZnO has been widely used in various applications such as transparent conductive oxide electrodes, solid state lighting, piezoelectric devices, gas sensors, and in bio-detection [31, 21].

### 2.11.3 ZnO Electronic Band Structure

ZnO energy band gap has been reported by many calculations based on a local density approximation (LDA), on a density functional theory (DFT), or on a self-interaction corrected pseudo-potentials method (SIC-PP) [30]. Fig. 2.16 shows the LDA calculations of a ZnO electronic band structure. The structure is shown along the high symmetry lines ($c$) in the hexagonal Brillouin zone [30]. Both the valence band maxima and the lowest conduction band minima occur at k = 0.0 at the Γ-point [35]. The first two conduction band states are strongly Zn localized and correspond to empty Zn-3s levels. The bottom 10 bands occurring at (-9.0 eV) correspond to Zn-3d levels. The next 6 bands from (-5.0 eV to 0.0 eV) correspond to O-2p bonding states [35]. The band gap for ZnO has been calculated as 3.77 eV [33] which overestimates the experimental value of 3.37 eV [36]. The 0.3 eV difference in a band gap is due to the interaction effect of defects in experimental values. The

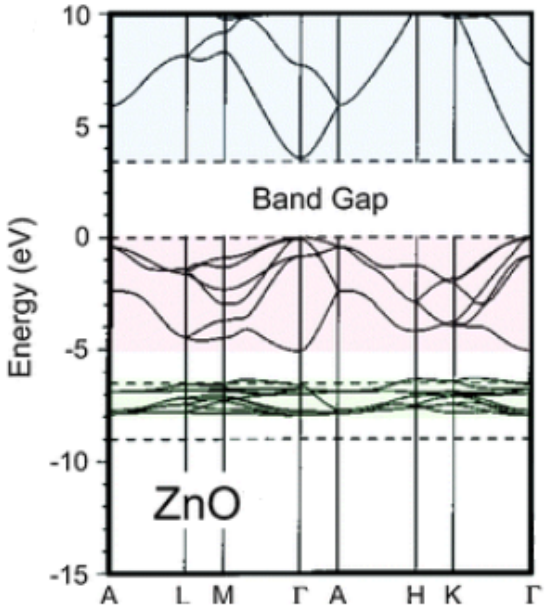


Figure 2.16: Calculated band structure of wurtzite ZnO using a local-density approximation [30].

most of the calculations agree that the lowest energy defects are oxygen and zinc vacancies [36].

### 2.11.4 ZnO Optical and Transitions Properties

Optical properties of ZnO are of a great interest to opto-electronic applications due to its wide band gap of 3.37 eV at room temperature with a large exciton energy of 60 meV, and the efficient radiative recombination [37]. The strong exciton binding energy is larger than GaN (25 meV), and the thermal energy at room temperature (25 meV) ensures an efficient exciton emission at room temperature under low excitation energy [38]. As a consequence, ZnO is recognized as a promising photonic material in blue ultraviolet (UV) regions. This properties are very useful for the development of many optoelectronic devices in applications as UV excitonic lasers, tuneable UV photo-detectors, and LEDs [37]. Optical and transitions properties of ZnO have been studied by different experimental techniques such as transmission, reflection, spectroscopic ellipsometry, photo reflection, optical absorption, photo-luminescence, calorimetric spectroscopy and cathode luminescence [39]. ZnO spectrum consists of an ultraviolet (UV) emission band and a broad emission band between the range of 300 nm and 800 nm [40, 37]. The UV emission band is dominated by free exciton (FE) emission. The UV peaks are generally observed

from the transition recombinations of free exciton (FE) near the band-edge of ZnO. Further details will be discussed in chapter 6.

### 2.11.5 Defects and Emission Properties of ZnO

A defect is defined as deviations from the perfect atomic arrangement such as missing ions, substituted ions, and interstitial ions [38] as shown in Fig. 2.17. Defect can occur in solids and metals. In general, defects can be categorized into three types:

i. point defects,

ii. line defects, and

iii. complex defects [37, 31].

The line defect occurs due to the disruptions into the rows of the atoms, where the point defects are generated due to the isolated atoms in localized regions and complex defects were formed when more than one point defects have merged [41]. Furthermore, the extrinsic point defects are generated if impurities atoms are incorporated in the structure. Intrinsic defects comprise only changes of host atoms [42]. ZnO crystal structures have typically two main types of intrinsic vacancy defects. These two main types are recognized as oxygen-vacancy (V-O) and zinc vacancy (V-Zn) [37]. These two main types have been previously attributed to deep level emission bands in the crystal structure but another defects such as oxygen-interstitial (O-i) [37] and zinc-interstitial (Zn-i) as well as extrinsic impurities can be present as shown in Fig. 2.15. The optical and electrical properties of ZnO can be altered due to the changes in the deep level defects of the ZnO crystal structure [40]. These defects can occur during a fabrication process or by applying other techniques such as ion implantation, atomic layer deposition, and post annealing [37].

## 2.12 Synthesis of ZnO

### 2.12.1 Bottom-up Process

A bottom-up fabrication is the process of stack of atoms on each other onto the substrate which gives a rise to crystal planes. Crystal planes further stack onto each other resulting in the synthesis of whole layer structure [36]. This process can be

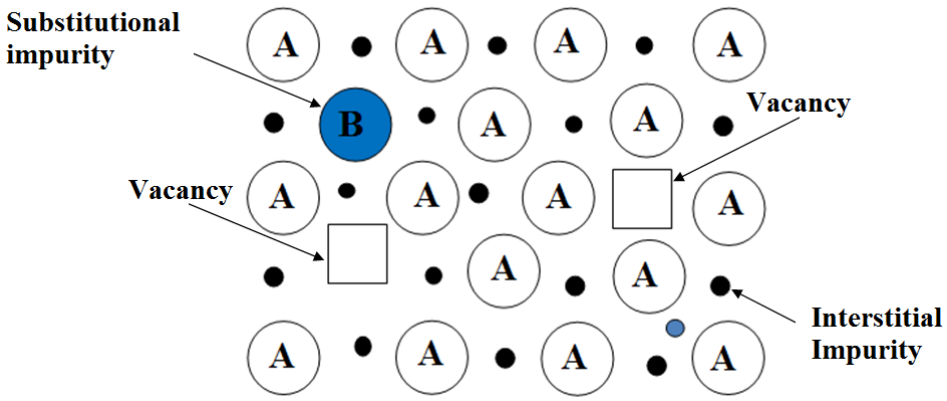


Figure 2.17: A schematic showing the defect types in crystal structure.

described as a synthesis approach where building blocks are added onto a substrate to form the nano-structures [31].

The bottom-up fabrication process can be done using chemical vapour deposition (CVD) or hydrothermal techniques [36]. These processes often need a catalyst to increase the rate of chemical reactions [43] and the most common catalyst used is Au [44]. The size of the catalyst defines a diameter of NWs [45]. The catalyst also guides NWs which are normally identified by the epitaxial orientation that results in alignment of the growth [46]. Moreover, one of the most common advantages of bottom-up growth methods is a production of a high crystalline morphology and a large aspect ratio [47]. However, there are some disadvantages which can be listed as follow:

i. a difficult control of the NW length at large-scale dimensions [47];

ii. a random alignment on device substrate which limits the control over nano-wire locations [48].

Various studies have demonstrated novel nano-devices using different materials such as InAs, GaN [31]. ZnO NWs bottom-up grown method have recently demonstrated a high performance [50]. Fig. 2.18 (a and b) shows a scanning electron microscopy (SEM) of ZnO NWs after hydrothermal growth. Fig. 2.18(b) demonstrates that the NWs are covering all the surface area which indicates a better deposition at the surface [34]. Furthermore, Fig. 2.18 (c) shows a cross-section of ZnO around the surface. The inset confirms the single crystalline structure of the ZnO NWs [34]. Fig. 2.18 (d) shows an atomic force microscopy image of grown NWs with Al source and drain contacts.

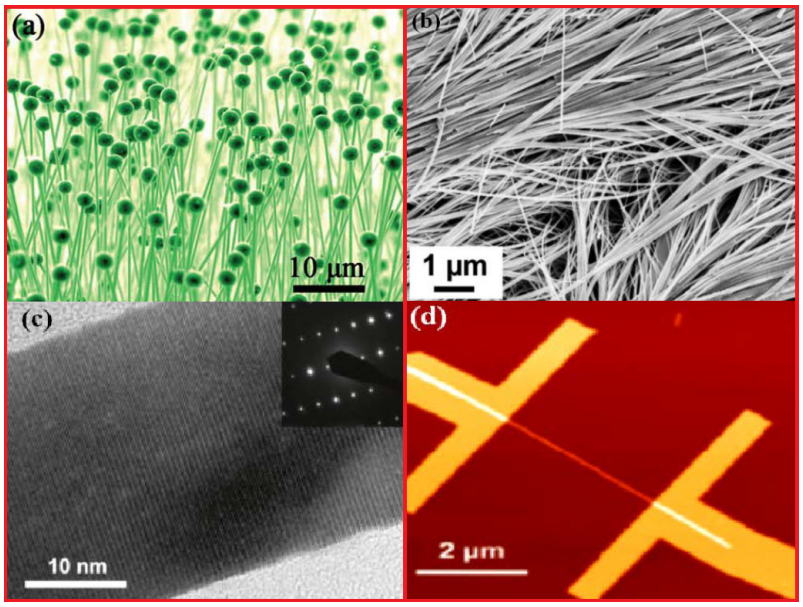


Figure 2.18: (a) Scanning electron microscopy image of ZnO NWs synthesized by a vapour liquid solid (VLS) method [49]. (b) Scanning electron microscopy of a dense carpet of ZnO NWs after a hydrothermal growth. (c) Transmission electron microscopy image of one of ZnO NWs grown by a hydrothermal growth. The inset confirms the single crystalline structure of the ZnO NWs. (d) Atomic force microscopy image of an as-grown NWs with Al source and drain contacts [47].

### 2.12.2 Top-Down Process

A top-down fabrication can be defined as the approach where building blocks are removed from substrate to form a nano-structure [18]. A top-down approach such as electron-beam lithography and deep ultra-violet (DUV) can be used to fabricate ZnO NW field effect transistors (FETs) and ZnO thin-film transistors (TFTs). This technique would use a Si wafer as a substrate for the growth [35]. Electron-beam lithography uses a direct pattern-writing with an electron beam with a widths down to 10 nm [35]. This process has a slow writing speed which makes it impractical for a large-scale manufacturing [41]. On the other hand, the DUV lithography is an expensive process because it requires advanced photo-resists and a light source [39]. The top-down fabrication might use a sacrificial oxide deposition and etch the sacrificial oxide in order to form pillars which can be used as an insulator between wires and transistors [41]. This approach is a very effective process to grow ZnO NWs in order to identify the location and to control dimensions of NWs [39]. Fig. 2.19 shows ZnO NW arrays formed after a sacrificial oxide etch. A width and a height of the ZnO NWs are about 10 nm and 90 nm, respectively. The SEM image also shows the array of ZnO NWs etched into a Si wafer [39].

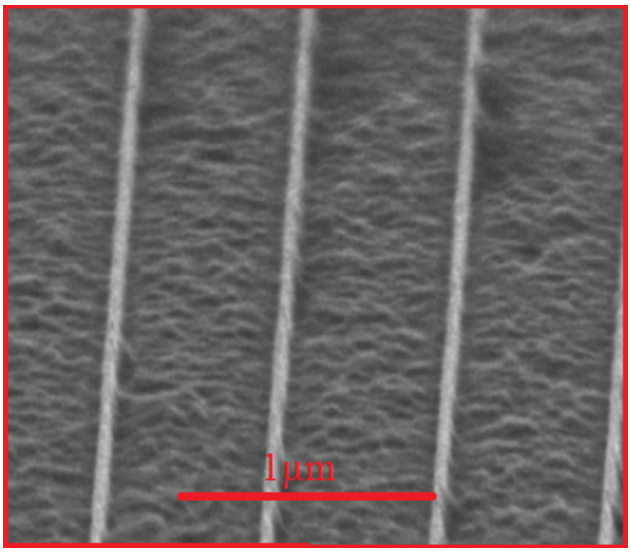


Figure 2.19: SEM image of ZnO nanowire array fabricated by a top-down fabrication method [45].

### 2.12.3 ZnO Film Deposition

Many deposition techniques have demonstrated a growth of highly crystalline ZnO films at low temperature [34]. Table 2.2. shows the various thin-film growth techniques and their properties used to produce ZnO thin films at different growth temperatures. A thin-film deposition is widely used in several areas such as fabrication of electronic semiconductor devices, LEDs, hard coatings on cutting tools, magnetic recording media, and optical coatings [43]. The process depends on many factors such as thickness, diameter and temperature of reaction [31, 43]. Furthermore, thin film growth technique shows a great impact on the electrical characteristics such as contact resistance and electron mobility [34]. Some technique requires a high temperature because of pure control of impurities during a growth [37]. Table 2.2 illustrates that electron carrier concentration of ZnO single crystal growth can be in the range between $10^{13}$ to $10^{20}$ $cm^{-3}$. This electron carrier concentration can increase due to the increase in a growth temperature (as the temperature increases, the number of carriers increases because there is a more thermal energy available and, therefore, more electrons gain kinetic energy [41]. Table 2.2 shows also that a Hall mobility is in the range between 100 to 155 $cm^2/Vs$. This value is a relatively large compared to those obtained from other growth techniques such as thermal growth [41]. However, these values are lower compared to the ZnO single crystal growth (200 $cm^2/Vs$) which is due to a low temperature and a smaller carrier concentration used in a single crystal growth [34]. Based on the results in Table 2.2, the

atomic layer deposition (ALD) is an attractive technique because of ZnO thin-film can be deposited at temperatures below 100°C which is close to the room temperature [40, 47]. The carrier concentrations and Hall mobility obtained from the samples grown by the ALD can be modulated with deposition temperatures to obtain semiconducting properties without deposition treatments such as annealing in air [34]. The ALD offers several advantages over the other techniques such as large area uniformity, effective growth control of the thickness, and composition of the thin films [41].

### 2.12.4 ZnO Thin Film Transistors

A thin film transistor (TFTs) is a type of field-effect transistors [18]. If a ZnO TFT is being developed for display applications, the wide band gap of ZnO (3.4 eV) offers a desirable level of transparency. The common fabrication method for these devices is the top-down fabrication method. The common substrate normally used for ZnO TFTs is a silicon substrate (Si) because of the cost of Si material [31]. Table 2.2 shows electrical characteristics of TFTs recently fabricated by different research groups. The field effect mobility obtained from these ALD fabricated ZnO TFTs has values between 0.43 $cm^2$/Vs to 80 $cm^2$/Vs [51]. However, the ALD technique has some disadvantages such as low deposition temperature which will increase a defect level that results in deterioration of the interface quality. Another disadvantage of ALD is the decrease in carrier concentration due to the formation of oxygen vacancies which reduces carrier mobility [32].

### 2.12.5 ZnO Nanowire Field-Effect Transistors

ZnO NWs have demonstrated outstanding performances due to their special material properties and wide-range device applications [51]. ZnO NWs field-effect transistors (FETs) have shown to operate with enhanced operation speed in nano-scale electronics [61]. ZnO NW FET fabrication requires a synthesis method which can produce a high quality and a good performance of ZnO devices [30]. Many growth techniques have been developed for a better diameter control, aspect ratio, and crystalline structure [32]. The growth of NWs provides mostly a single crystal with lengths reaching micrometers within a short time of synthesis reaction [33].
In general, ZnO NW FETs can be produced by either vapour solution phase growth,

Table 2.3: Survey of various ZnO thin film deposition techniques, and the extracted mobility demonstrated by different research groups.

| Sample | Growth temperature°C | Carrier Conc. ($cm^{-3}$) | Mobility $cm^2V^{-1}s^{-1}$ | Ref. |
|---|---|---|---|---|
| Sol-gel process using PLD grown on Si $_2$/Si substrate | 350 - 400 | N/A | 0.30 | [52] |
| Spray pyrolysis grown on Si $_2$/Si substrate | 400 | $1\times10^{17}$ | 25 | [53] |
| Thermally Oxidized grown on glasses substrate | >300 | N/A | 5.3 - 13.6 | [54] |
| Pulsed laser deposition grown on SiN/Si substrate | 300 | N/A | 7 | [55] |
| Rf magnetron sputter deposition grown on glasses | 300 - 600 | N/A | 20 - 50 | [56] |
| Plasma enhanced CVD grown on $SiO_2$/Si substrate | 300 | N/A | 18.2 - 29.6 | [57] |
| PLD: ZnO thin film on sapphire substrates | 750 | $25\times 10^{16}$ | 115 - 155 | [41] |
| MBE:ZnO thin film on MgO buffered sapphire substrates | 700 | $1\times10^{17}$ | 130 | [40] |
| MOCVD:ZnO thin film grown on sapphire | 600 | $4\times 10^{17}$ | 24 | [50] |
| SPUTTER:ZnO thin film on glass | RT | $3\times 10^{16}$ | 2.0 | [47] |
| ALD: ZnO thin film grown on SiO $_2$/Si | 70 - 130 | $1\times 10^{14}$ $1\times1$ $^{19}$ | 6.4 - 152 | [37] |
| ALD: ZnO thin film grown on SiO $_2$/Si substrate | 70 - 250 | $1\times 10^{13}$ $1\times10^{20}$ | 0.43 - 22 | [42] |
| Pulsed laser deposition grown on SiO $_2$/Si substrate | 400 | N/A | 40 | [58] |
| RF magnetron sputtering grown on $Ta_2O_5$/Si substrate | RT | N/A | 50 | [59] |
| Vapor phase deposition grown on SiO $_2$/Si substrate | 1200 | N/A | 0.3 - 0.6 | [60] |

Table 2.4: Review of ZnO NWFET electrical performance.

| Method | Growth treatment °C | $\mu$(cm$^2$/Vs) | $V_{Th}$ (V) | SS (V/dec) | $I_{on}/I_{off}$ | Ref. |
|---|---|---|---|---|---|---|
| Bottom-up | Polyimide passivation | 75 - 1000 | -21 - 0.3 | 0.2 - 3.37 | $10^4$ - $10^6$ | [61] |
| Bottom-up | None | 13 | -12.5 | N/A | $10^5$ - $10^7$ | [33] |
| Bottom-up | $SiO_2/Si_3N_4$ passivation | 30-3118 | -10-18 | 0.15 - 3 | $10^3$- $10^4$ | [32] |
| Bottom-up | Air annealing | 928 | 0.4 | 0.129 | $10^6$ | [30] |
| Bottom-up | $SiO_2/Si_3N_4$ passivation | 30 - 3118 | -10 - 18 | 0.15 - 3 | $10^3$ - $10^4$ | [51] |
| Bottom-up | Air annealing | 70 - 1175 | -0.25 - 0.13 | 0.13 - 0.23 | $10^3$-$10^7$ | [38] |
| Bottom-up | PMMA passivation | 28-68 | -12.5-8.9 | 0.5 - 1 | $10^4$ - $10^6$ | [50] |
| Bottom-up | Laser anneal | 12.3 | -0.7 | 1.17 | $10^4$ | [43] |
| Bottom-up | $Ga^+$ irradiation | 36.7 - 34.5 | -105 - 8.1 | 1 | $10^7$ | [40] |
| Bottom-up | Air anneal | 36.7 - 34.5 | 0.09 - 0.4 | 1 | $10^7$ | [41] |
| Bottom-up | $H_2O_2$ treatment | 34.1 - 81.3 | -27 - 7.33 | 0.2 - 0.25 | N/A | [13] |
| Bottom-up | Ambient anneal | 6 | -2 | 0.5 | $10^6$ | [42] |
| Bottom-up | 10 NWs array | 80 | -7.5 | 0.7 | $10^5$ | [15] |

chemical vapour deposition (CVD), metal organic chemical vapour deposition (MOCVD), plasma enhanced chemical vapour deposition (PECVD), or vapour solid (VS) mechanism [32]. These fabrication methods will be discussed in more details later in Chapter 5. Based on the results in Table 2.3, the top-down fabrication of ZnO NWs needs a various treatments such as passivation and annealing in order to achieve desired electrical characteristics. This is because ZnO NWs have a large amount of surface defects as oxygen vacancies that will adsorb gas species and act as scattering and trapping centres leading to a lower carrier mobility [38].

## 2.13 Conclusion

In this chapter, a formation of metal-semiconductor contact was reviewed. Schottky barrier height and theory related to the origin of the barrier height as well as Ohmic contacts were discussed. The study also defined assumptions of forming an ideal interface between metal and semiconductor in a metal contact. This includes the description of a band gap diagram and a current transport mechanism across the interface such as emission over and through the barrier.

We have also explained the operation of MOSFETs as a conducting semiconductor

channel with two ohmic contacts (source and drain) where the number of charge carriers in the channel is controlled by a third contact (the gate). Furthermore, transmission line method (TLM) has been discussed in details. The TLM method is aimed to explore the capability to calculate a contact resistance and solve some physical problem of semiconductor devices.

The recent trends of semiconductor devices such as fabrication and scaling down are also discussed in this chapter. Requirements on operational speed, functionality, reliability, and costs of semiconductor devices are growing allowing for information technology to be dramatically improved. Due to these requirements and fabrication costs, semiconductor companies are increasing their research and development scope. Since we focus on the field effect transistors, the most distinct issue is device scaling down because this scaling can deliver all the requirements like operational speed, functionality, reliability, and costs. The scaling down executed to increase device performances and decreases fabrication cost induces unintended short channel effects which degrades performance of the scaled semiconductor transistors and thus requires to take radical recovery measures in transistor architectures.

In this chapter, a various fabrication techniques such as bottom-up and top-down have been presented. A bottom-up approach provides a cheap solution for mass production, because of its self-assembly process. In addition, nano-fabrication of semiconductor devices can be controlled by the bottom-up fabrication. However, a uniformity of device fabrication may not be homogeneous because of the randomness of molecular behaviour during the process. On the other hand, a uniformity and homogeneity, which might enhance device performance, can be achieved using the top-down fabrication. Most of the recent device fabrications are carried out with lithography technique using the top-down fabrication. This approach is a key to a next generation fabrication technology.

Moreover, a literature review of ZnO properties have been presented in this chapter. We have undergone through properties of chemical bonding, electronic band structure, physical, optical, defect and emission properties, with a summary of mobility values and other material characteristics reported in previous studies.

# References


[1] W. Eicke and R. K. Willardson. *The basic physics of intersubband transitions, in Intersubband transitions in quantum wells: Physics and Device Applications*. Vol. 62. Elsevier, 2000 (cit. on pp. 7, 8).

[2] S. Adachi. *Properties of Semiconductor Alloys: Group-IV, III-V and II-VI Semiconductors*. John Wiley and Sons, 2009 (cit. on pp. 7, 9, 11, 14).

[3] M. Di Ventra. *Electrical Transport in Nanoscale Systems*. Vol. 14. Cambridge University Press, 2008 (cit. on pp. 7, 8, 10).

[4] J. L. Freeouf and J. M. Woodall. "Schottky barriers: An effective work function model". In: *Electronic Structure of Metal Semiconductor Contacts*. Springer, 1990, pp. 154–156 (cit. on pp. 7, 11).

[5] M. Ameri, F. Boufadi, A. Touia, M. Faudil, D. Hachemane, K. Boudia, A. Slamani, and A. Aze-Eddine. "Ab Initio Calculations Study of Structural and Electronic Properties of Ternary Alloy $Al_xIn_{1-x}As$". In: *Materials Sciences and Applications* 3.10 (2012), p. 674 (cit. on p. 8).

[6] J. P. Heida, B. J. Van Wees, J. J. Kuipers, T. M. Klapwijk, and G. Borghs. "Spin orbit interaction in a two-dimensional electron gas in a InAs/AlSb quantum well with gate-controlled electron density". In: *Physical Review B* 57.19 (1998), p. 11911 (cit. on pp. 9, 13, 14).

[7] E. O. Kane. "Band structure of indium antimonide". In: *Journal of Physics and Chemistry of Solids* 1.4 (1957), pp. 249–261 (cit. on pp. 9, 14).

[8] V. Palankovski, G. Kaiblinger-Grujin, and S. Selberherr. "Study of dopant dependent band gap narrowing in compound semiconductor devices". In: *Materials Science and Engineering: B* 66.1 (1999), pp. 46–49 (cit. on p. 9).

[9] *International technology Roadmap for semiconductors*. http://public.itrs.net. Accessed: 2015-06-30 (cit. on pp. 10, 13, 16, 18).

[10] E. K. U. Gross and R. M. Dreizler. *Density functional theory*. Vol. 337. Springer Science and Business Media, 2013 (cit. on pp. 10, 23, 24).

[11] S. H. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi. "High performance InAs on insulator n-MOSFETs with Ni-InGaAs S/D realized by contact resistance reduction technology". In: *Transactions on Electron Devices* 60.10 (2013), pp. 3342–3350 (cit. on p. 13).

[12] M. Aldegunde, S.P. Hepplestone, P.V. Sushko, and K. Kalna. "Multi scale simulations of a Mo/$n^+$GaAs Schottky contact for nano-scale III-V MOSFETs". In: *Semiconductor Science and Technology* 29.5 (2014), p. 054003 (cit. on p. 13).

[13] R. Anderson. "Experiments on Ge-GaAs heterojunctions". In: *Solid State Electronics* 5.5 (1962), pp. 345–351 (cit. on pp. 13, 36).

[14] K. Kalna, N. Seoane, A. J. Garcia-Loureiro, I. G. Thayne, and A. Asenov. "Benchmarking of scaled InGaAs implant-free nano MOSFETs". In: *Transactions on Electron Devices* 55.9 (2008), pp. 2297–2306 (cit. on p. 13).

[15] Y. Fedoryshn. "Modeling, growth and characterization of InGaAs/AlAsSb quantum well structures for all optical switching based on inter sub-band transitions". PhD thesis. Lviv Polytechnic National University, Ukraine, 2012 (cit. on pp. 14, 36).

[16] K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen, H. S. Kim, C. Liu, Y. Chueh, E. Plis, S. Krishna, H. Bechtel, J. Guo, and A. Javey. "Quantum confinement effects in nanoscale thickness InAs membranes". In: *Nano Letters* 11.11 (2011), pp. 5008–5012 (cit. on p. 15).

[17] Y. Taur and H. T. Ning. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, New York, 1988 (cit. on pp. 15, 17–20).

[18] M. L. Hitchman and K. F. Jensen. *Chemical vapour deposition: principles and applications*. Vol. 79. New York, 2016 (cit. on pp. 15, 26, 32, 34).

[19] X.and Lim S. K. Brewster M. M.and Zhou and S. Gradeccak. "Role of Au in the Growth and Nanoscale Optical Properties of ZnO Nanowires". In: *Journal of Physics Chemistry Letter* 2.6 (2011), pp. 586–591 (cit. on pp. 16, 17).

[20] *International technology Roadmap for semiconductors*. http://public.itrs.net. Accessed: 2015-06-30 (cit. on p. 16).

[21] S. M Sze and K. K. Ng. *Physics of semiconductor devices*. John Wiley and Sons, 2006 (cit. on pp. 17–20, 24, 27, 28).

[22] F. Leonard, D. Lonard, A. Talin, B. Swartzentruber, and S. Picraux. "Diameter-Dependent Electronic Transport Properties of Au-Catalyst/Ge-Nanowire Schottky Diodes". In: *Physics Review Letters* 10.102 (2009), p. 106805 (cit. on pp. 18–21).

[23] A. Ortiz-Conde, F. J. Garcia Sänchez, and J. Juin. "On the extraction of threshold voltage, effective channel length and series resistance of MOSFETs". In: *Journal of Telecommunications and Information Technology* (2000), pp. 43–58 (cit. on pp. 18–20).

[24] A. Ortiz-Conde, F. Sánchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue. "A review of recent MOSFET threshold voltage extraction methods". In: *Microelectronics Reliability* 42.4 (2002), pp. 583–596 (cit. on p. 20).

[25] Y. Yunxiang, M. Stanislav, C. Binjie, S. M. Z. Anis, L. Xiaoyan, and C. Asen. "Back Gate Bias Dependence of the Statistical Variability of FDSOI MOSFETs With Thin BOX". In: *Transactions on Electron Devices* 60.2 (2013), pp. 739–745 (cit. on pp. 21, 22).

[26] A. Srivastava. "Back gate bias method of threshold voltage control for the design of low voltage CMOS ternary logic circuits". In: *Microelectronics Reliability* 40.2 (1999), pp. 2107–2110 (cit. on p. 22).

[27] G. K. Reeves and H. B. Harrison. "Obtaining the specific contact resistance from transmission line model measurements". In: *Transactions on Electron Devices* 3.5 (1982), pp. 111–113 (cit. on p. 22).

[28] Z. Chen and J. Appenzeller. "Mobility extraction and quantum capacitance impact in high performance graphene field-effect transistor devices". In: *IEDM Tech. Dig.* IEEE. 2008, pp. 1–4 (cit. on pp. 24, 25).

[29] H. H. Berger. “Models for contacts to planar devices”. In: *Solid State Electronics* 15.2 (1972), pp. 145–158 (cit. on p. 25).

[30] C. Jagadish and S. J. Pearton. *Zinc oxide bulk, thin films and nanostructures: processing*. Elsevier, 2006 (cit. on pp. 26, 28, 29, 34, 36).

[31] E. Ludmila. *Physics of Thin Films*. Vol. 1. Springer, 1977 (cit. on pp. 26–28, 30, 31, 33, 34).

[32] Z. L. Wang. “Zinc oxide nanostructures: growth, properties and applications”. In: *Journal of Physics Condensed Matter* 16.4 (2004), pp. 829–858 (cit. on pp. 26, 34, 36).

[33] C. Klingshirn. “ZnO: From basics towards applications”. In: *Physica Status Solidi: b* 244.9 (2007), pp. 3027–3073 (cit. on pp. 26–28, 34, 36).

[34] Ü Özgür, Y. I. Alivov, C. Liu, A. Teke, M. Reshchikov, S. Doğan, V. Avrutin, S. J. Cho, and H. Morkoc. “A comprehensive review of ZnO materials and devices”. In: *Journal of Applied Physics* 98.4 (2005), p. 11 (cit. on pp. 26, 27, 31, 33, 34).

[35] S. J. Pearton, D. P. Norton, K. Ip, Y. W. Heo, and T. Steiner. “Recent progress in processing and properties of ZnO”. In: *Progress in Materials Science* 50.5 (2005), pp. 293–340 (cit. on pp. 28, 32).

[36] S. Singh, P. Thiyagarajan, M. Kant, D. Anita, S. Thirupathiah, B. Rama N.and Tiwari, M. Kottaisamy, and M. S. Ramachandra-Rao. “Structure, microstructure and physical properties of ZnO based materials in various forms: bulk, thin film and nano”. In: *Journal of Physics D: Applied Physics* 40.9 (2007), pp. 6312–6327 (cit. on pp. 28–31).

[37] M. T. Borseth, G. B. Svensson, and Y. A. Kuznetsov. “Identification of oxygen and zinc vacancy optical signals in ZnO”. In: *Applied Physics Letters* 89.4 (2006), p. 262112 (cit. on pp. 29, 30, 33, 35).

[38] P. Klason, T. M. Borseth, Q. X. Zhao, B. G. Svensson, A. Y. Kuznetsov, P. J. Bergman, and M. Willander. “Temperature dependence and decay times of zinc and oxygen vacancy related photoluminescence bands in zinc oxide”. In: *Solid State Communication 145* 89.4 (2008), pp. 321–326 (cit. on pp. 29, 30, 36).

[39] B. Lin, Z. FU, and Y. Jia. “Green luminescent center in undoped zinc oxide films deposited on silicon substrates”. In: *Applied Physics Letters* (2001), pp. 943–945 (cit. on pp. 29, 32).

[40] T. S. Jeong, M. S. Han, J. H. Kim, S. J. Bae, and C. J. Youn. “Optical properties of BeZnO layers studied by photoluminescence spectroscopy”. In: *International Journal of Modern Physics: D* 40.4 (2007), p. 370 (cit. on pp. 29, 30, 34–36).

[41] J. Wu and S. C. Liu. “Low-temperature growth of well-aligned ZnO nanorods by chemical vapor deposition”. In: *Advanced Materials* 14 (2002), pp. 215–218 (cit. on pp. 30, 32–36).

[42] Z. L. Wang. “Nanostructures of Zinc Oxide”. In: *Materials Today* 7.6 (2004), pp. 26–33 (cit. on pp. 30, 35, 36).

[43] D. Florescu, L. G. Mourok, F. H. Pollack, D. C. Look, G. Cantwell, and X. Li. "High spatial resolution thermal conductivity of bulk ZnO (0001)". In: *Journal of Applied Physics* 91.4 (2002), pp. 890–892 (cit. on pp. 31, 33, 36).

[44] S. T. Ho, K. C. Chen, A. H. Chan, Y.H. Lin, Y. C. Cheng, and N. H. Lin. "Catalyst-Free Surface-Roughness-Assisted Growth of Large-Scale Vertically Aligned Zinc Oxide Nanowires by Thermal Evaporation". In: *Chemistry of Materials* 19.9 (2007), pp. 4083–4086 (cit. on p. 31).

[45] W. I. Park, D. H. Kim, S. W. Jung, and G. C. Yi. "Metalorganic vapor-phase epitaxial growth of vertically well-aligned ZnO nanorods". In: *Applied Physics Letters* 33.2 (2002), pp. 4232–4234 (cit. on pp. 31, 33).

[46] G. T. Wang, A. A. Talin, J. D. Werder, J. R. Creighton, E. Lai, Anderson, R. J., and I. Arslan. "Highly Aligned, Template-Free Growth and Characterization of Vertical GaN Nanowires on Sapphire by MetalOrganic Chemical Vapour Deposition". In: *Nanotechnology* 17.6 (2006), pp. 5773–5780 (cit. on p. 31).

[47] F. M. Ross. "Controlling Nanowire Structures through Real Time Growth Studies". In: *Reports on Progress in Physics* 73.4 (2010), p. 114501 (cit. on pp. 31, 32, 34, 35).

[48] S. Ray and A. G. Shard. "Quantitative Analysis of Adsorbed Proteins by X-ray Photoelectron Spectroscopy". In: *Analytical Chemistry* 83.22 (2011), pp. 8659–8666 (cit. on p. 31).

[49] Y. Dongshan, T. Trad, T. Jr, T. J. McLeskey, C. Valentin, and R. Taylor. "ZnO Nanowires Synthesized by Vapor Phase Transport Deposition on Transparent Oxide Substrates". In: *Nanoscale Research Letters* 5.8 (2010), pp. 1333–1339 (cit. on p. 32).

[50] S. K. Tiku, C. K. Lau, and K. M. Lakin. "Chemical vapor deposition of ZnO epitaxial films on sapphire". In: *Applied Physics Letters* 36.4 (1980), pp. 318–320 (cit. on pp. 31, 35, 36).

[51] Y. Xiu-Tian and X. Yongdong. *Introduction to Chemical Vapour Deposition. In: Chemical Vapour Deposition. Engineering Materials and Processes*. Vol. 79. Springer, 2010 (cit. on pp. 34, 36).

[52] C. George. "Fabrication and Comparison of ZnO Thin Film Transistors with Various Gate Insulators". In: *Journal Of Electronic Review* 1.9 (2006), pp. 34–35 (cit. on p. 35).

[53] R. L. Hoffman. "ZnO-channel thin-film transistors: Channel mobility". In: *Jornal of Applied Physics* 95.10 (2004), pp. 5813–5819 (cit. on p. 35).

[54] Kang H. Jinhua L. Shanshan L. Yun G. Wei T. Xiaojun G. Jianying W. Tao M. Xianbao W. Li J. "High carrier mobility low-voltage ZnO thin film transistors fabricated at a low temperature via solution processing". In: *Ceramics International* 1.9 (2018), 11751–11756 (cit. on p. 35).

[55] Faruque M. H. Shingo T. Tetsuya A. Koji S. Yuji O. Isao O. Shuya K Ak O. Tomoteru F. Fumihiro M. Yuzo O. Hideomi K. Hideo O. Masashi K. Junya N. "High Mobility Thin Film Transistors with Transparent ZnO Channels". In: *Japanese Journal of Applied Physics* 42.4 (2018), 347–349 (cit. on p. 35).

[56] Wager J. F. Hoffman R. L. Jeong J. Keszler D. A. Chianga H. Q. “High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer”. In: *Applied Physics Letters* 86.9 (2005), p. 013503 (cit. on p. 35).

[57] Horng-Chih L. Pei-Wen L. Chin-I K. “Improving the Performance of ZnO Thin-Film Transistors with ZnON Source/Drain Contacts”. In: *Transaction On Electron Devices* 64.7 (2017), 2849–2853 (cit. on p. 35).

[58] George V.-Christopher S. William-I. M. George A. Mazran E. “High-Mobility ZnO Thin Film Transistors Based on Solution-processed Hafnium Oxide Gate Dielectrics”. In: *Advanced Functional Materials* 25.9 (2015), 134–141 (cit. on p. 35).

[59] Jidong J.-Yi L. Peng-B. Aimin M. S. Christian B. “Sputtered ZnO Thin-Film Transistors With Carrier Mobility Over 50 $cm_2$/Vs”. In: *Transaction On Electron Devices* 60.10 (2013), 3424–3428 (cit. on p. 35).

[60] Gen-Wen H. Sharvari-D. Marcus C. N. James E. S. Pritesh H. Arokia N. Paul A. W. Husnu U. Paul B. Andrew J. F. Ian R. Gehan A. William I. M. Flora M. . “Zinc Oxide Nanostructures and High Electron Mobility Nanocomposite Thin Film Transistors”. In: *Transaction On Electron Devices* 55.11 (2008), 3001–3010 (cit. on p. 35).

[61] A. Wei, X. W. Sun, J. X. Wang, Y. Lei, X. P. Cai, C. M. Li, Z. L. Dong, and W. Huang. “Enzymatic glucose biosensor based on ZnO nanorod array grown by hydrothermal decomposition”. In: *Applied Physics Letters* 89.4 (2006), p. 123902 (cit. on pp. 34, 36).

# Chapter 3

# Methodology and Characterisation Techniques

## 3.1 Introduction

The chapter provides details on methodology and characterisation techniques. The understanding of fundamental reactions of chemical vapour deposition (CVD) use to grow ZnO NWs will be discussed in this chapter. This includes a CVD process and set-up, CVD reactors, substrate loading mechanism, growth rate, nucleation and the key growth parameters affecting the CVD reaction.

The characterisation techniques described in this chapter used in this thesis are the scanning electron microscopy (SEM) and the energy dispersive X-ray (EDX), the X-ray photo-electron spectroscopy (XPS), and photo-luminescence (PL) in order to investigate the chemical composition and optical properties of ZnO NWs. Their working principles used to analyse morphology and chemical characterization of ZnO NWs will be discussed as well. In addition, a technical details of four point probes measurement used to investigate the electrical characteristics will be introduced.

## 3.2 CVD Grow and Reaction Set-Up

The technique can relies on the gases which are transported into a reaction chamber for a deposition [1]. The precursor gases (carrier gases) delivered into the reaction chamber come into a contact with a heated substrate. This reaction forms a solid phase deposited onto the substrate [2]. These steps can be illustrated briefly into

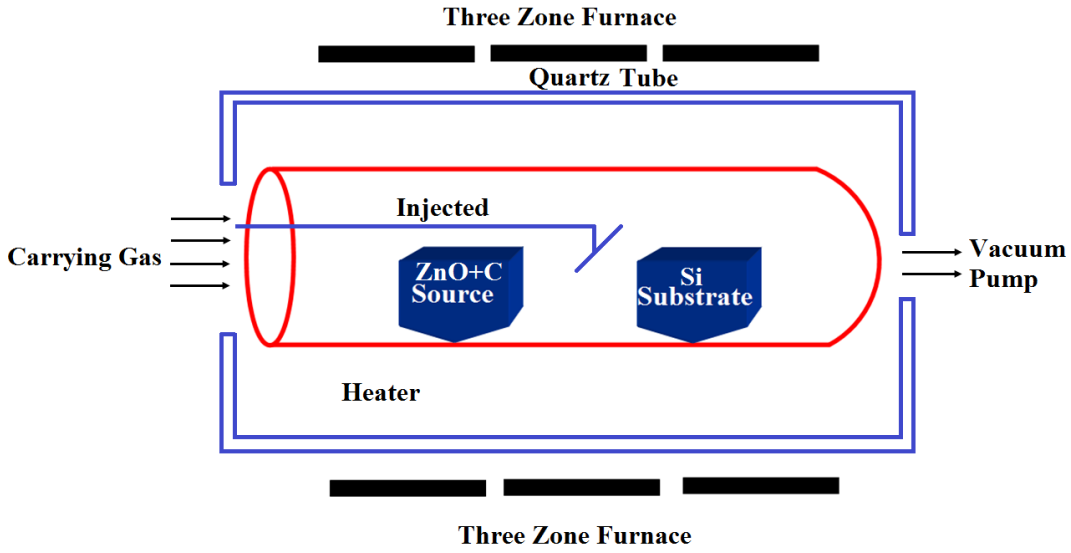


Figure 3.1: Schematic diagram of CVD apparatus. Reaction gas is supplied on one end of the apparatus, and gas outlet on the other end.

five steps:

i. precursors or the evaporation operation and transport of reagents in the bulk gas flow region into the reactor,

ii. gas phase reactions of precursors in the reaction zone to produce reactive intermediates and gaseous by-products [1],

iii. mass transport of reactants to a surface substrate ,

iv. adsorption of reactants on a surface substrate,

v. surface diffusion to growth sites, nucleation and surface chemical reactions leading to a film formation,

vi. desorption and mass transport of remaining fragments of decomposition away from reaction zone [2].

The temperature in a reaction chamber has to be closely monitored as it plays a major role in reactions. Fig 3.1 shows the basic principle of CVD of flowing a precursor gases into a chamber which contains a substrate to be coated [3]. Chemical reactions can occur on the hot surfaces and result in a deposition of a thin film on the surface [3].

### 3.2.1 Reactant Transport

This is a flow of the reactants through the CVD chamber. A main objective of the reactant is to deliver the gas uniformly to a substrate [4]. The liquid flow has to be optimized for a maximum deposition rate. The liquid flow can be a gas diffusion or viscous (liquid flow). In this case, CVD takes place in the viscous regime [4]. The reactant can also occur if the flow take the following rate:

i. low flow rates produce laminar flow (desired),

ii. high flow rates produce turbulent flow (avoided).

Reactants in a gas delivery system including diluent, extender, and carrier gases must be transported and metered in a controlled manner into a reactor. In the case of gaseous reactants, this cannot present any particular problem and it is accomplished by a pressure controllers, gauges, flow meters, and mass-flow controllers [1].

### 3.2.2 Chemical Vapour Deposition Reactors

The reactor chamber takes control of reaction regime in a CVD reaction. In a reaction-controlled regime, a deposition rate is very sensitive to reaction temperature [1]. In a diffusion-controlled regime, there are two types of a chamber control. One type is a hot wall system which acts like a furnace, where is the heat can be controlled by a furnace [5] as illustrated in Fig. 3.2. A film deposition occurs only on the walls of a chamber. The second type is a cold wall system which acts like a furnace. In this furnace system, the wafers lie flat on a susceptor (typically made of graphite) which is inductively heated. This type of a chamber has a poor temperature control but no deposition on wall chambers. The wall chambers are tilted to keep boundary layer thickness constant [5]. In addition, the choice of the reactor is determined by the application requirements, for example, material substrate, material coating and morphology, film thickness and uniformity, availability of precursors, and cost. These two reactor types will be now described in details [1].

#### Hot Wall Reactor System

Hot wall reactors are one of the main categories of CVD reactors. The reactor tube is surrounded by a furnace tube which makes substrate and wall reactor to be at the same temperature. A large number of substrates can be coated in this type of

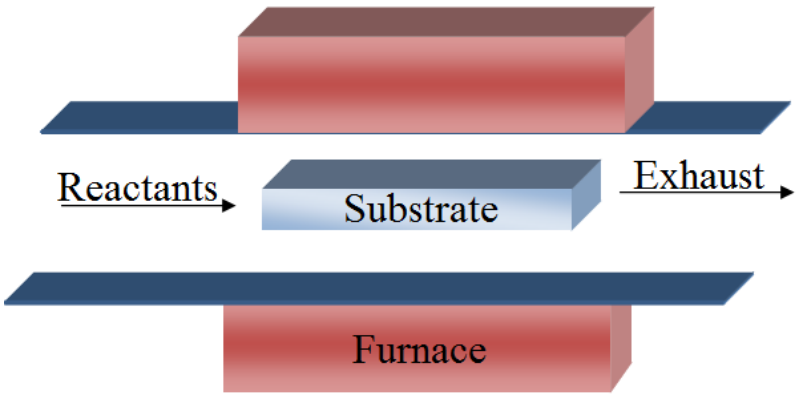


Figure 3.2: Schematic shows the hot wall CVD reactor.

reactor. The main drawback of this type of reactor is deposition on the reactor wall and a possible contamination in the system from chemical reactions between the reactor wall, and a vapour due to a high temperature of the reactor wall. Therefore, the hot wall reactor is ideal for the case where the reaction is exothermic since the high wall temperature prevents undesirable deposition on the reactor walls [1]. Fig. 3.2 shows a schematic for a hot walled reactor depicting a specialized support which holds a large number (over a hundred) of closely-spaced silicon wafers for simultaneous processing [2].

In general, the hot wall reactors have many advantages of being able to process large batches of substrates, to hold a relatively uniform substrate temperature and thus achieve an uniform coating thickness [1]. However, the disadvantage of hot walled reactor is that the walls are very heavily coated. This heavy coat requires a frequent cleaning which might causes problems with uniformity on deposited surfaces. Addition to the hot wall reactors require a higher thermal load and a large energy usage which is costly [2].

### Cold Wall Reactor System

The second type of a CVD reactor is a cold wall reactor, where the substrates are heated but the walls are cooled [2]. In the cold wall reactor, only the susceptor where the substrates are placed is intentionally heated by RF induction, or high radiation lamps. This type of reactor is predominantly used for deposition reactions which are endothermic, such as Si deposition from the halides. Since the substrates have

a higher temperature than the reactor wall, the reaction will proceed most readily on the hot surface of the substrate.

In this reactor type, the contamination due to the interaction between the reactor wall and the vapour can be greatly reduced. Frequently the walls are water cooled to prevent deposition on the wall or reactions between walls and vapour. The cooling of a system is achieved by a water-cooled quartz walls with a rotating holder for (silicon or compound semiconductor) wafers that is resistively heated from below [5]. A cold wall reactor often runs at relatively high pressures and usually have reactive precursors diluted in a carrier gas [1]. One sub-type of cold-walled reactors is a lamp heated single-wafer reactor which is widely used in microelectronics fabrication. The other sub-type is inductively heated horizontal flow reactor [5]. A cold wall reactor has advantage of reducing the deposition of material on the walls which then requires a less cleaning, a lower thermal load on the substrates because of faster heat-up and cool-down times, a lower energy consumption, and avoidance of vacuum equipment [2]. The main disadvantages of cold walls reactors are: a larger temperature of the processing leading to a larger non-uniformity on the substrate and thus to non-uniformity in a film thickness, smaller batch sizes, and possible thermal stress on the substrates if the heating/cooling is too rapid [5].

A specialized variation of a cold walled reactor is the continuous reactor shown schematically in Fig. 3.3. In this system, the surface to be coated moves underneath of a set of gas injectors and is heated from below [6]. In some cases, the substrates (wafers) are placed on a belt moving over a set of rollers. In other cases, such as the large-scale application of optical coatings to glass, the moving belt could be the float-glass sheet itself. These systems are essentially open to atmosphere, the reactive gases are contained by curtains of inert gas on either side of the deposition zone [4].

### 3.2.3 Substrate Loading Mechanism

Substrate loading mechanism is positioned for placing uncoated substrates in the inner deposition chamber and for removing a coated substrate from the inner deposition chamber [7]. The operation can be protected from exposure to elevated temperatures. In this position, dust and gas generating surfaces can be easily isolated from the wafer boats and inner deposition reaction chamber parts. That

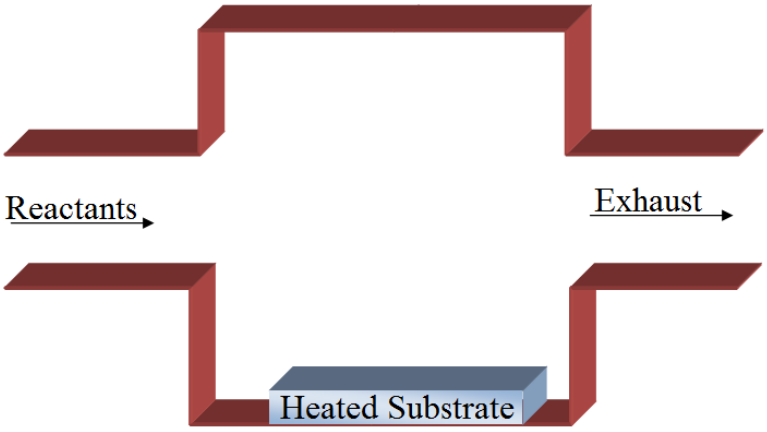


Figure 3.3: Schematic shows the cold wall CVD reactor.

arrangement can provide an efficient reaction chamber through the loading and unloading of substrates which does not contribute to contamination by dust or vapours to the deposition zone, therefore, substantially increasing the quality of the coated products [8]. Each substrate is loaded into a receiving chamber upon a positionable platform. The platform is positioned from the receiving chamber into the feed chamber where the substrates are off loaded. A cassette containing stacked substrates can be loaded upon the platform to transport substrates into the feed chamber.

### 3.2.4 Energy Source

There are several types of energy source for heating in the CVD processes. These types include: resistive heating (tube furnaces), radiant heating (halogen lamps), radio frequency heating (induction heating), and other photo energy sources such as UV-visible light or lasers [2].

### 3.2.5 Vacuum System

A CVD process is generally performed in an effective vacuum condition. There are two main factors that affect the CVD vacuum condition:

i. removal or minimisation of active atmospheric constituents, that could cause physical or chemical reactions [8],

ii. improvement of the coating uniformity by increasing the free path of precursor gases. As the pressure is decreased from its atmospheric value, the sources of

gases in a vacuum system are free to move. Therefore, a free mean path increases which results in improvement in the coating uniformity [2].

Most CVD systems operate in the low or medium vacuum regimes. In order to express the state of a vacuum system, we have to consider undesirable gases existing in the system to reflect a dynamic equilibrium during pumping process. These can be summarised into:

i. gas molecules of the initial atmosphere enclosed in the vacuum system [8],

ii. gas which penetrates into the system as a result of leakage.

Taking into consideration the above factors, the influence of various gas sources on the vacuum system during the operation of CVD must be taken into account [2].

### 3.2.6 Exhaust System

The exhaust pressure can be defined as the pressure at the outlet of the vacuum pump system. Vacuum pumps are generally divided into 13 categories due to working principles [9]. The categories include, water jet pump, water ring pump, steam ejector, oil-sealed rotary pump, root pump, vacuum diffusion pump, oil vapour booster pump, sputtering-ion pump, radial field pump, titanium sublimation pump, absorption pump, molecular pump, and cryo-pump system for removal of volatile by-products from the reaction chamber [2].

### 3.2.7 Growth Rate

Arrhenius plot can be used to describe the growth rate in three regimes. In other words, the Arrhenius plot shows the transition between the mass transport limited growth rate and the surface kinetics limited growth rate depending on the temperature regime [10]. Mass transport limits reactions at high temperatures and surface reaction kinetics dominates at low temperatures where the growth rate increases with temperature at a constant pressure of reactants [4]. Feed rate limited reactions are independent of temperature because the rate of gas delivery is only factor to limit a reaction.

Fig. 3.4 shows Arrhenius plot of the dependence of CVD growth rate as a function of the temperature [7]. There are three regions. The first region is at lower growth

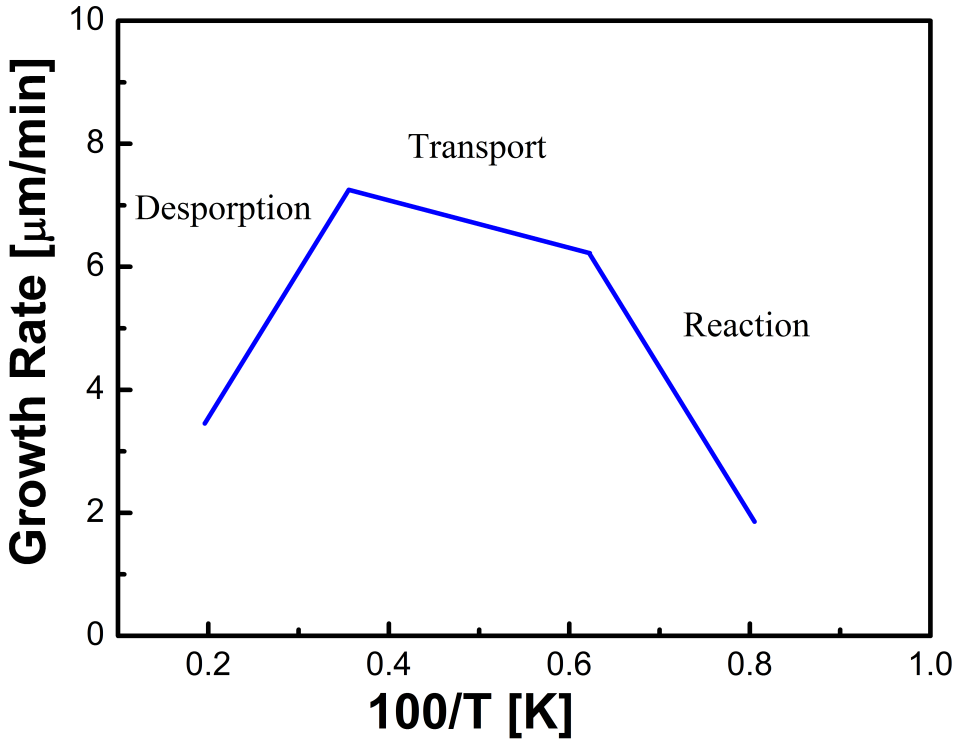


Figure 3.4: Arrhenius plot of the dependence between CVD deposition rate and temperature.

temperatures (surface reaction limited). The growth rate is normally controlled by the kinetics of chemical reactions on the surface substrate [4]. The second region is a diffusion or a mass transport limited, when a gas transport increases with the temperature increase. This improves deposition and growth on the surface. The third region is at higher temperature. The film growth rate becomes almost independent of temperature and the growth is determined by a mass transport of precursors through the boundary layer to the growth surface [10].

### 3.2.8 Nucleation Growth

A nucleus and thermodynamic growth play important role in the CVD process. These nucleations and growth process are the fundamental and important factor in the optimization of film quality and corresponding control of film physical properties [11]. The CVD reaction can exist in two types of nucleation:

i. homogeneous: nucleus is formed in vapour form before being deposited and do not incorporate into the crystal structure of the film [12],

ii. heterogeneous: nucleus is formed on a substrate and incorporated into the film

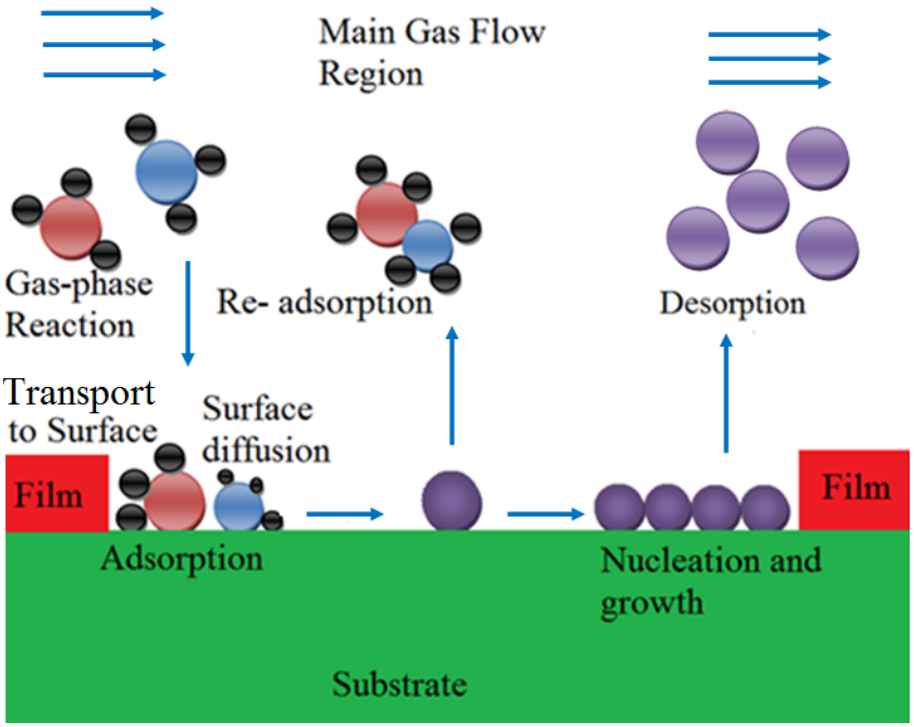


Figure 3.5: Precursor transport, nucleation growth and reaction processes in CVD.

structure resulting in a more easy growth [13].

Fig 3.5 shows the basic process of CVD reaction and nucleus growth. A growth time of (45 minutes-one hour) is standard for ZnO NWs CVD growth [11]. We have examined the sample grown over different times. Samples were placed in the furnace for growth times of 45 minutes confirming a good quality of ZnO NWs. When ZnO powder is mixed and placed in the reaction chamber, the entire powder mix is consumed due to re-deposition of ZnO on the surface with carbon forming an impermeable layer. If the furnace operates for 45 minutes, Zn and O start to interact together till the reaction is completed. Fig. 3.5 shows a basic princip of the reaction.

### 3.2.9 Film Deposition

Film deposition closely relates to the flow of the gas over the substrate. Deposition is determined by adsorption and reaction rates [9]. The deposition rate and quality of the deposition are affected by the factors as a distance from gas inlet, specifics of the reaction, and radial variance [2].

### 3.2.10 The Key Growth Parameters Affecting Domain Structure of CVD

There are several parameters affecting the domain structure of CVD [11]. These parameters can be categorised according to the reactors type:

i. pressure – CVD can be carried out at atmospheric pressure or under a low pressure,

ii. precursor decomposition – the energy supplied to initial chemical reaction can be delivered in the form of heat, light, RF, plasma or another method,

iii. number of precursors – the amount of precursors which form bonds in the film,

iv. precursor transport – to introduce the gas phase via heating, liquid injection or through the formation of a vapour,

v. type of reaction chamber – a hot/cold wall, and a horizontal/vertical/dynamic substrate [1].

Fig. 3.5 shows a precursor transport and reaction process in CVD used to grow ZnO NWs on a Si substrate.

## 3.3 Experimental Techniques

### 3.3.1 Scanning Electron Microscope

A scanning electron microscope (SEM) is an electron microscope which can be used to produce an image for the sample [14]. SEM consists of the following components:

i. electron source which includes an electron gun at the top, the column down which the electron beam travels, and the sample chamber at the base,

ii. electron detector for all signals of interest,

iii series of lenses within a vacuum chamber,

iv. sample stage and computer to divert the signal into the microscope, with the additional bench controls [2].

To study the working principle of the SEM: When the sample hits by incident beams, the electron interacts with the atom in sample, therefore, the emitted X-rays forms a three types of electrons which are primary backscattered electrons, secondary electrons and Auger electrons [15]. These electrons usually penetrated the sample to a depth of a few microns, depending on the accelerating voltage and the density of the sample. And finally the microscope enables information to be collected by one or more detectors to form images which are then displayed on the computer screen. SEM also reveals details about a morphology of the a sample [16]. If the electron hits the sample, thermionic gun heats a filament until electrons stream away [16]. The field emission rips electrons away from their atoms by generating a strong electrical field. Then the lenses reflect/direct the electrons towards the specimen in order to maximize efficiency [15]. An electron recorder picks up the rebounding electrons and records their imprint. This information is translated onto a screen which allows images to be represented [17]. The maximum resolution obtained in an SEM depends on multiple factors, like the electron spot size and interaction volume of the electron beam with the sample. Fig. 3.6 shows a schematic diagram of the fundamental components of SEM. The electron gun forms a source of electrons which are accelerated towards the anode. These electrons pass through one or more electron lenses (magnetic, electrostatic, crossed field, multiple, mini, maxi, and superconducting) and the image of the electron source is formed in the plane of the specimen after successive reductions with a diameter of a few tenths to a few tens of nanometres [12].

The SEM used in this thesis is Hitachi S 4800 cold field emission gun. The field emission source offers a high resolution (1-2 nm) and excellent performance operation over wide range of operation of acceleration voltages about (0.5-30 kV) and a magnification up to 800 kx, with YAG BSE backscatter detector of resolution 3 nm Oxford instruments 50 $mm^2$ EDX detector [17].

### 3.3.2 Energy Dispersive X-Ray

Energy-dispersive X-ray spectroscopy (EDX) is an analytical technique used to probe the composition of a solid materials [17]. Each element has a unique atomic structure allowing a unique set of peaks on its electromagnetic emission spectrum. Measuring these emissions can provide both qualitative and quantitative informa-

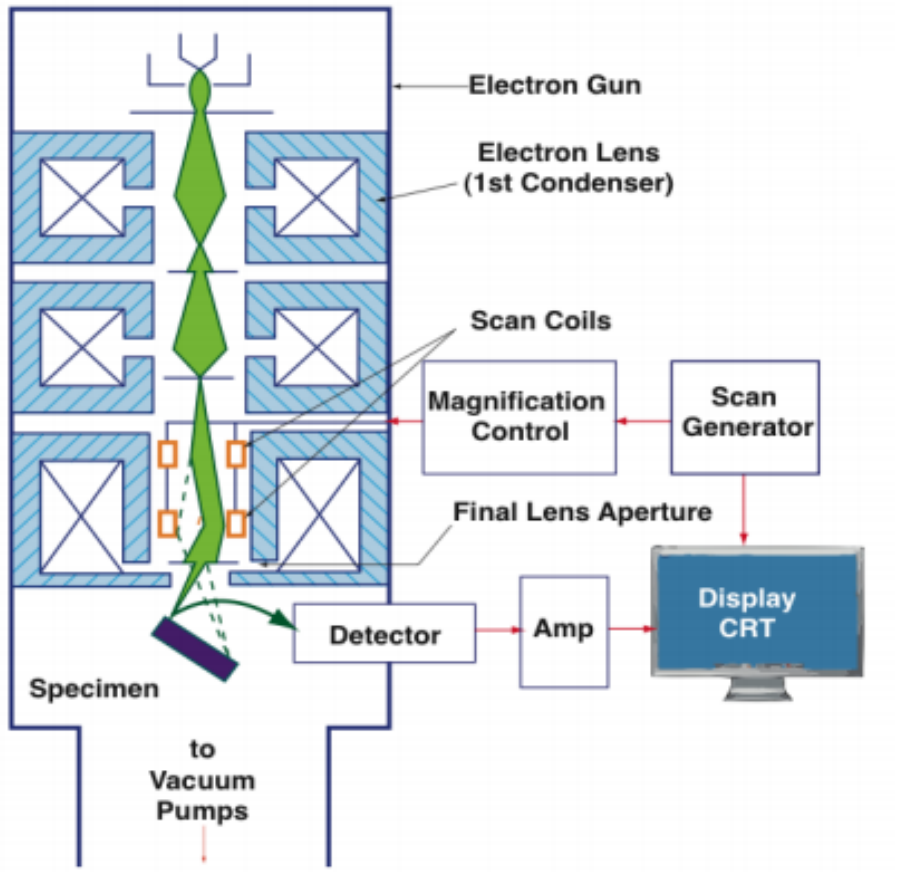


Figure 3.6: (a) Shows a schematic diagram of the fundamental components of SEM. (b) The basic process of SEM steps [17].

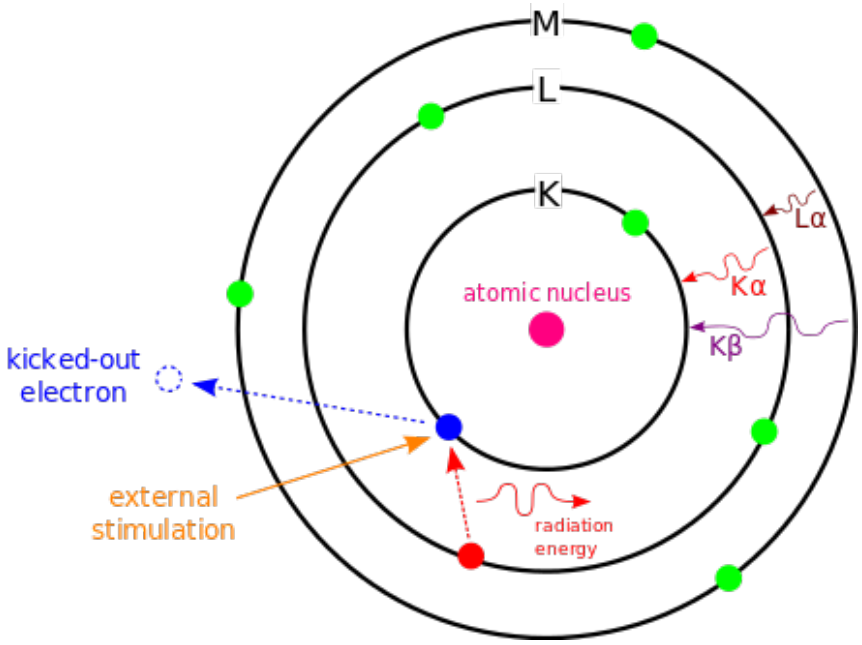


Figure 3.7: Schematic diagram shows an atoms core shells and basic principles of EDX [15].

tion about the near-surface of the sample [2]. For the working principal, when the sample hits by the electron beam, electrons are ejected from the atoms comprising the sample surface. The resulting electron vacancies are filled by electrons from a higher state, and an X-ray is emitted to balance the energy difference between the two electrons states[17]. Then X-ray energy is a characteristic of the element from which it was emitted [15]. Finally, the EDX detector measures the relative abundance of emitted X-rays versus their energy. From quantum mechanical model for atoms, the energy state of electron inside atom can be defined by a set of quantum numbers. If the primary quantum numbers ($n$) provides the coarsest description of the electrons energy level, and all the sub-levels that share the same primary quantum number comprises an energy shell in atom. It can be clearly described that, the lowest-energy shell as the ($n = 1$ shell), is more common in spectroscopy use an alphabetical labels, whereas, the $K$ shell has $n = 1$, the $L$ shell has $n = 2$, the $M$ shell has $n = 3$ [15]. Subsequent quantum numbers divide the shells into sub-shells, one for $K$, three for $L$, and five for $M$ as it shows in Fig. 3.7.

### 3.3.3 X-Ray Photo-electron Spectroscopy

X-ray photo-electron spectroscopy (XPS) is a surface analytical technique based on photo-ionization effect [18]. In principle, when the X-ray beam illuminates the

surface of a specimen, the core electron of the atom on the surface will absorb the entire X-ray photon energy. If the X-ray photon energy is large enough, the core electron will escape from the atom and emit out of the surface with certain kinetic energy [19], which is also called a photo-electron energy as it shows in Fig. 3.8. Because the energy of an X-ray with particular wavelength is known and the emitted electrons kinetic energies are measured, therefore, the electron binding energy of each emitted electrons can be determined by using an equation.

$$E_b = E_{photon} - (E_k + \phi) \tag{3.1}$$

where $E_b$ is the binding energy, $E_k$ is the kinetic energy, $\phi$ is the work function of the spectrometer, and $\nu$ is the frequency of the radiation. This relation is based on the work of Ernest Rutherford (1914) where is $E_{photon} = h\nu$ [15]. Therefore, the kinetic energy $E_k$ of these photoelectrons is given by:

$$E_k = h\nu - E_b - \phi \tag{3.2}$$

Since we know the X-ray photon energy and the work function $E_w$, the kinetic energy is only determined by the binding energy. An electron located at each atomic orbital has its unique binding energy [19]. Each element excited by X-ray will exhibit a set of peaks which depends on the kinetic energy in the XPS spectrum. Therefore, we normally plot the XPS spectrum as a function of binding energy instead of kinetic energy [19]. Most of the elements can be identified by measuring the binding energy of their electron core. This can be represented as peaks at particular energies which indicates the presence of a specific element in the sample [18].

A chemical reaction can extremely influence the binding energy of electron core. The shift of the corresponding peaks can then be used to study chemical status of elements at the surface [19]. The peak intensity of XPS spectrum determines the concentration of corresponding elements within the surface. Thus XPS peaks can be used to calculate the chemical composition percentage of the sample [18]. The SEM used in this thesis is a Kratos Supra XPS, which an Ocean optics USB 2000+ spectrometer.

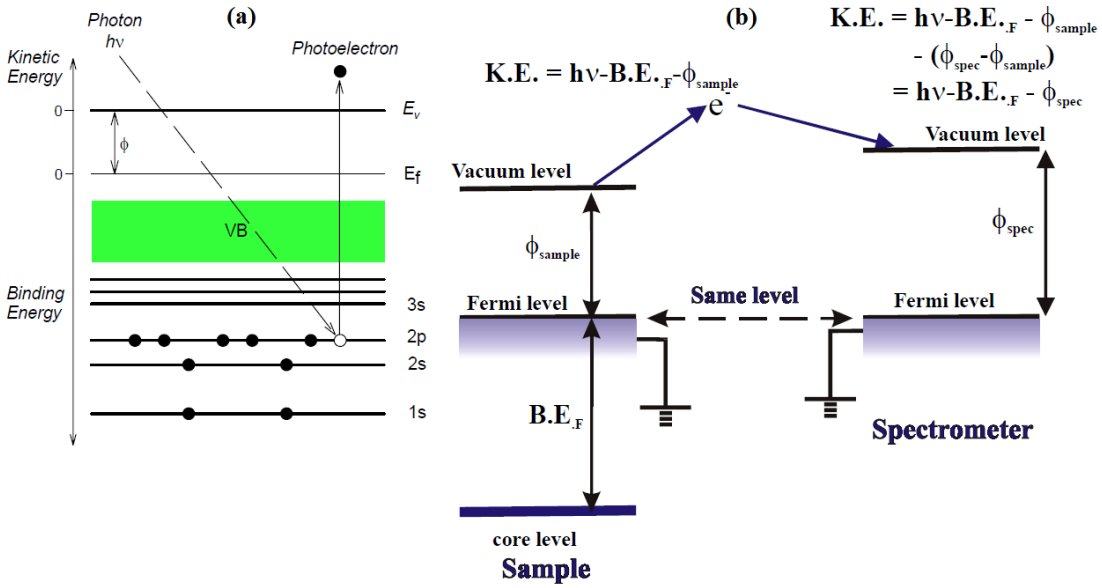


Figure 3.8: Schemes for (a) soft X-ray emission spectroscopy showing the atomic orbital distribution inside the molecules and (b) soft X-ray photo-electron spectroscopy of sample showing the binding energy exhibiting a set of peaks depended on kinetic energy in the XPS spectrum.

### 3.3.4 Photo-luminescence

Photo-luminescence (PL) is an optical emission triggered by photon excitation, typically in III-V semiconductor materials [18]. This type of analysis allows non-destructive characterization of semiconductors and it can also investigate the qualitative composition of sample [7].

The photo excitation causes electrons within the material to move into permissible excited states. When the electrons return to equilibrium states, the excess energy is released. This includes the emission of the light as shown in Fig. 3.10 (a and

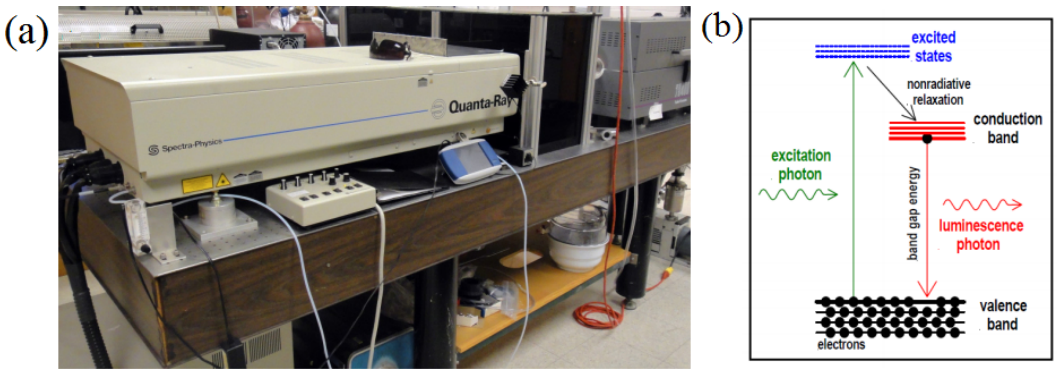


Figure 3.9: (a) A photo-luminescence based contact-less gas sensing set-up, (b) energy diagram showing absorption of light and the processes involved in the emission of light as fluorescence and phosphorescence.

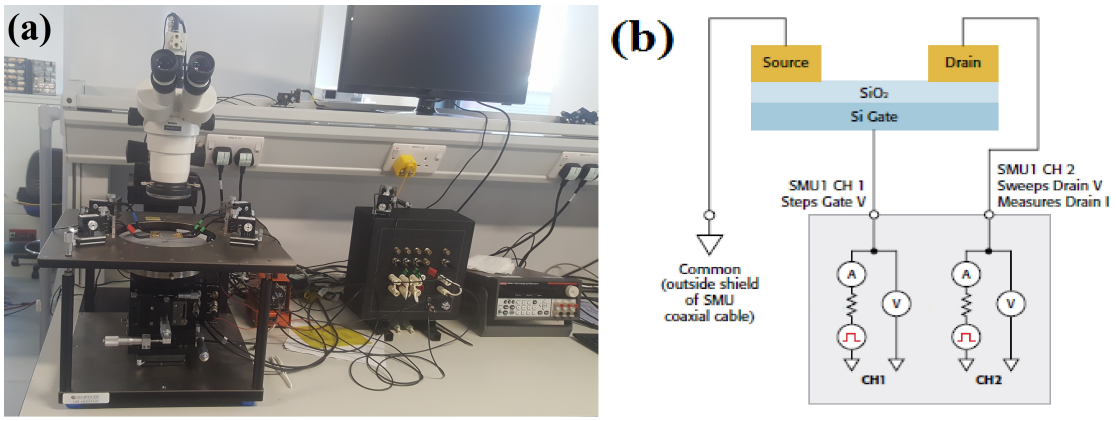


Figure 3.10: (a) Four point probe system, (b) schematic diagram of equivalent circuit of a four-point probe connected to three terminals.

b). The energy of the emitted light is related to the difference in energy levels between two electron states involved in the transition between the excited state and the equilibrium state [18]. If the energy of photons coming from the laser source is greater than the energy gap of the semiconductor, the sample emits photon [7]. The PL used in this thesis is an Ocean optics using a Melles-Griot 325 nm He-Cd laser as the excitation source.

### 3.3.5 Four point probes measurement

The four-probe method works by contacting the metal probes to a material or device terminals. The schematic in Fig. 3.11 (a and b) shows a four point probe system [20]. Since a transistor has 3 terminals: the source, the gate, and the drain, only three probes are needed. A direct current (DC) is applied between the two probes (the source and the drain), while one probe is needed to test the third terminal. A typical test configuration for connecting the simultaneous measure unit 2 (SMU. 2) and (SUM. 2) module to the source and the gate with a ground contact to be the source is shown in Fig. 3.11(b). In this diagram, channel 1 (Ch. 1) of the SMU. 2 is connected to the gate terminal and channel (Ch. 2) is connected to the drain terminal. in order to obtain ($I_D$-$V_D$) characteristics, Ch. 1 steps the gate voltage and Ch. 2 sweeps the drain voltage and measures the resulting drain current [21].

#### Four Point Probes Measurement Steps

The measurement has been taken by use the Ossila software, and follow these steps:

i. place the sample on the stage, centred under the four-point probe. Use a

micrometre to raise the stage until probes are in a good contact with a sample. As the probes are spring-loaded, they will compress as a sample is raised into them - creating a constant contact force.

ii. Then set up appropriate range on the source-measure unit (SMU. 1),

iii. ensure that the same range is set physically on the system as is selected in a software,

iv. click a measure button, the system will apply the set target current between the outer two probes. Once this has been achieved, the voltage will be measured between the inner two probes and the sheet resistance calculated from these values.

iiv. Once a measurement has finished, the results will be displayed on computer window.

## 3.4 Conclusion

The overall aim of this chapter is to study the methodology and characterisation techniques used in this thesis. The understanding of fundamental reactions of chemical vapour deposition (CVD), such as reactant transport, CVD reactors, substrate loading mechanism, energy source, vacuum system, exhaust system, film deposition, growth rate, nucleation, mass transport, CVD reactor types and the key growth parameters affecting the CVD reaction, that allows a deepen knowledge have been described in details.

The characterisation techniques used in this thesis and their working principles are also discussed in this chapter. A description of scanning electron microscopy (SEM) and energy dispersive X-ray (EDX), which were used to provide elemental identification and quantitative compositional information of the sample, have been also included. These two techniques have therefore been recently used in order to assess and investigate the physical and chemical properties of ZnO NWs.

X-ray photo-electron spectroscopy (XPS) used to provide a chemical details of ZnO NWs is discussed, as well as the photo luminescence (PL) used to provide a crystalline and high purity of ZnO NWs. A deep understanding of these analytical techniques allows us to study NWs structures and their properties in large details.

Finally, a four probes equipment used to investigate the electrical characterisation has been described in this thesis. The description provides comprehensive details of using four point probe method for measuring electrical characteristics. The experimental set up consists of: probes arrangement, sample, and constant current generator. This equipment is one of the standard and most widely used for semiconductor devices measurements of I-V characteristics, carrier mobility and carrier sheet density.

# References


[1] M. L. Hitchman and K. F. Jensen. *Chemical vapour deposition: principles and applications*. Vol. 79. Elsevier, 2016 (cit. on pp. 45–49, 54).

[2] G. Kumar, R. Kumar, and A. Kumar. "ZnO Thin Films: Chemical Vapour Deposition, Growth and Functional Properties". In: *Reviews in Advanced Sciences and Engineering,* 5.2 (2016), pp. 150–160 (cit. on pp. 45, 46, 48–51, 53, 54, 57).

[3] Ü. Özgür, Y. I. Alivov, C. Liu, A. Teke, M. Reshchikov, S. Dougan, V. Avrutin, S. J. Cho, and H. Morkoc. "A comprehensive review of ZnO materials and devices". In: *Journal of Applied Physics* 98.4 (2005), p. 041301 (cit. on p. 46).

[4] S. Singh, P. Thiyagarajan, M. Kant, D. Anita, S. Thirupathiah, N. Rama, B. Tiwari, M. Kottaisamy, and M. S. R. Rao. "Structure, Microstructure and Physical Properties of ZnO based materials in various forms: bulk, thin film and nano". In: *Journal of Physics D: Applied Physics* 40.9 (2007), pp. 6312–6327 (cit. on pp. 47, 49, 51, 52).

[5] M. S. Simon and K. N. Kwok. *Physics of semiconductor devices*. Vol. 79. John Wiley and Sons, 2006 (cit. on pp. 47, 49).

[6] C. Jagadish and S. J. Pearton. *Zinc Oxide Bulk, Thin Films and Nanostructures Processing, Properties and Applications*. Elsevier, 2006 (cit. on p. 49).

[7] M. F. Ross. "Controlling Nanowire Structures through Real Time Growth Studies". In: *Reports on Progress in Physics* 73.11 (2010), p. 114501 (cit. on pp. 49, 51, 59, 60).

[8] S. J. Pearton, D. P Norton, K. Ip, Y. W. Heo, and T. Steiner. "Recent progress in processing and properties of ZnO". In: *Progress in Materials Science* 34.2 (2003), pp. 3–32 (cit. on pp. 50, 51).

[9] P. Klason, T. M. Borseth, Q. X. Zhao, B. G. Svensson, P. J. Kuznetsov, and M. Willander. "Temperature dependence and decay times of zinc and oxygen vacancy related photoluminescence bands in Zinc Oxide". In: *Solid State Communications* 145.5 (2008), pp. 321–326 (cit. on pp. 51, 53).

[10] Z. L. Wang. "Zinc Oxide nanostructures: growth, properties and applications". In: *Journal of Physics: Condensed Matter* 16.4 (2004), pp. 829–858 (cit. on pp. 51, 52).

[11] J. Wu and S. C. Liu. "Low-temperature growth of well-aligned ZnO nanorods by chemical vapor deposition". In: *Advanced Materials* 14 (2002), pp. 215–218 (cit. on pp. 52–54).

[12] M. J. Zheng, L. D. Zhang, G. H. Li, and W. Z. Shen. "Fabrication and optical properties of large-scale uniform zinc oxide nanowire arrays by one-step electrochemical deposition technique". In: *Chemical Physics Letters* 363 (2002), pp. 123–128 (cit. on pp. 52, 55).

[13] A. Wei, X. W. Sun, J. X. Wang, Y. Lei, X. P. Cai, C. M. Li, Z. L., and W. Huang. "Enzymatic glucose biosensor based on ZnO nanorod array grown by hydrothermal decomposition". In: *Applied Physics Letters* 89.4 (2006), p. 123902 (cit. on p. 53).

[14] T. M. Borseth, B. G. Svensson, A. Y. Kuznetsov, P. Klason, Q. X. Zhao, and M. Willander. "Identification of oxygen and zinc vacancy optical signals in ZnO". In: *Applied Physics Letters* 89.26 (2006), p. 262112 (cit. on p. 54).

[15] E. Ludmila. *Physics of Thin Films*. Vol. 1. Springer, 1977 (cit. on pp. 55, 57, 58).

[16] G. Kumar, R. Kumar, and A. Kumar. "ZnO Thin Films: Chemical Vapour Deposition, Growth and Functional Properties". In: *Reviews in Advanced Sciences and Engineering,* 5.2 (2016), pp. 150–160 (cit. on p. 55).

[17] J. B. Cui. "Structural and optical properties of periodically ordered ZnO Nanowires". In: *Science in China Series E: Technological Sciences* 52.2 (2009), pp. 313–317 (cit. on pp. 55–57).

[18] P. K. Ghosh. *Introduction to Photoelectron Spectroscopy, Vol. 67 aus: Chemical Analysis: A Series of Monographs on Analytical Chemistry and its Applications*. Vol. 67. John Wiley and Sons, 1983 (cit. on pp. 57–60).

[19] S. Ray and A. G. Shard. "Quantitative Analysis of Adsorbed Proteins by X-ray Photoelectron Spectroscopy". In: *Analytical Chemistry* 83.22 (2011), pp. 8659–8666 (cit. on p. 58).

[20] V. Paul, R. J. Pesavento, C. R. Chesterfield, C. Newman, and F. Daniel. "Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature". In: *Journal of Applied Physics* 76.12 (2005), pp. 3027–3073 (cit. on p. 60).

[21] S. Keller, S. Mouaziz, G. Boero, and J. Brugger. "Microscopic four-point probe based on SU-8 cantilevers". In: *Review of Scientific Instrument* 96.12 (2004), pp. 1251021–1251025 (cit. on p. 60).

# Chapter 4

# Simulation Results and Discussion-Source/Drain Contact of Nano-Scale InAs nMOS

## 4.1 Introduction

In the literature review of chapter 2, III-V semiconductor compounds have demonstrated characteristics such as a high electron mobility and a large saturation velocity along the channel to eventually replace the current silicon channel in $n$-type transistors in complementary metal oxide semiconductors (CMOS) [1]. III-V semiconductors show a great advance to develop the basic fabrication processes needed for CMOS technology [2]. InAs exhibits outstanding injection electron velocity resulting in a reduced power dissipation at a low voltage operation because of its higher electron mobility than the mobility in Si [2]. However, there are still remaining challenges which need to be addressed to identify a satisfactory interface materials that can exhibit a low resistance for contacts in nanoscale channels based on III-V semiconductors [3].

This chapter presents a multi-scale simulation study of a nano-scale contact combining density functional theory (DFT) calculations with solutions of 1D Poisson-Schrödinger (1DPS) equation aiming to understand a relation among contact resistance and band structure at the interface. The ultra-low resistance nano-scale contact is of a great relevance to the future sub-10 nm technology [3].

The nano-scale contact is made of Ni metal interfacing with an 11-nm thick InAs

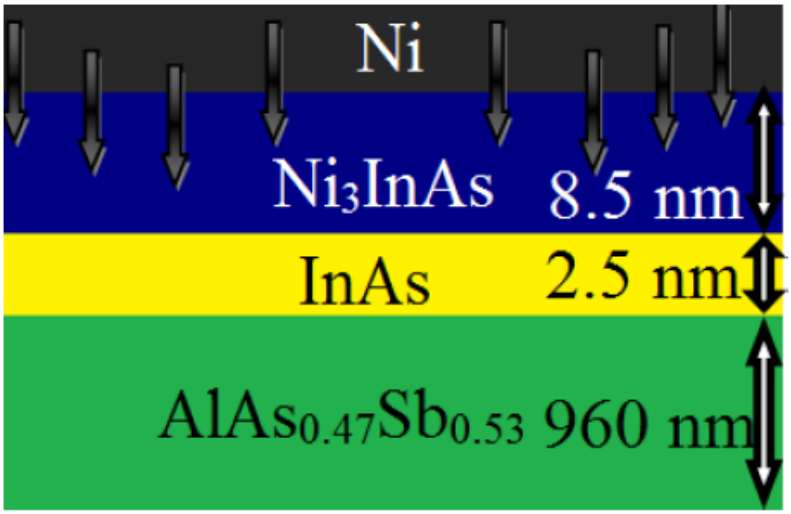


Figure 4.1: Schematic of layer structure for MOSFET. Structure has an 8.5 nm $Ni_3InAs$/2.5 nm InAs and $AlAs_{0.47}Sb_{0.53}$ layers. The $Ni_3InAs$ alloy is formed by Ni deposition on the 10 nm InAs layer.

layer on a *p*-type doped $AlAs_{0.47}Sb_{0.53}$ buffer. A thermal reaction between Ni and InAs results in a formation of the 8.5 nm thick $Ni_3InAs$ layer leaving only a 2.5 nm thick InAs acting as a channel [3]. The density functional theory (DFT) calculations have revealed a band-gap narrowing in the InAs at metal-semiconductors interface. The simulation results assuming the band-gap narrowing in the InAs give exceptionally good agreement with experimental [3] observation of a contact sheet resistance.

## 4.2 Nickel Contact for Source/Drain of III-V MOSFET

The development of III-V MOSFETs for the future sub-10 nm technology nodes for digital applications faces several challenges [3]. One of the most essential challenge is to demonstrate a low resistance interface between metal and semiconductor in nano-scale III-V technology [4]. The extensive investigations have shown that a self-aligned Ni contact can form nickelide-semiconductor compound having a low contact resistance in the source-drain area of III-V MOSFETs [4]. Building on the experiment demonstration of III-V heterostructure MOSFETs [5], the ternary compounds Ni, In, and As have been reported in several experimental studies as a crystalline, the study suggested that a combination between these materials is a

nickelide-semiconductor [6]. Indium arsenide (InAs) has been recently associated as a particularly commendatory channel material for the 10 nm technology node generation due to its high channel mobility [1]. Furthermore, the recent studies have shown a stable (nickelide) metallic phase formed by a reaction of nickel with InAs [3].

Ni has been successfully deposited as a metal contact on the 10 nm InAs channel layer to form the source-drain (S-D) contact followed by thermal treatment to result in an 8.5 nm thick NiInAs alloy layer, leaving only a 2.5 nm thickness of un-doped InAs layers shown in Fig. 4.1. The contact fabrication has used a highly doped contact region to $3\times10^{19}$ cm$^{-3}$ by a selective implant with Ni to form a high-quality metal-semiconductor interface [3]. The source/drain contact model used in the simulations is chosen to match the dimensions and composition of experiment structure made of a 10 nm thick InAs channel deposited on $p$-type $AlAs_{0.47}Sb_{0.53}$ buffer doped to $1\times$ $10^{16}$ cm$^{-3}$.

## 4.3 Density Functional Theory Calculations of the Structure

In order to gain a physical insight into carrier transport through the contact, we have employed 1D simulations using a self-consistently [7] coupled Poisson-Schrödinger (PS) equations and assuming a real-space dependent material parameters (band gap and affinity) obtained from ab-initio density functional theory (DFT) calculations [6].

In the DFT calculations, the $Ni_3InAs$/InAs (100) interface has been modelled as a periodic heterostructure shown in Fig. 4.2. The DFT calculations have been performed to a large size of the unit cell (consisting of 1127 atoms) using the Perdew, Burke and Ernzerhof [8] functional and the projected augmented waves method [9] using the Vienna Ab-initio Simulation Package (VASP) [9]. A $2\times$ $2$ $\times$ $1$ Monkhorst-Pack **k**-point set is used for the calculation with a cut-off of 500 eV. The density of states (DOS) for the semiconductor segment of the structure has been projected on the atomic layers of In and As [10] to create the Layered Projected Density of States (LPDOS). LPDOS is divided into sub-regions, along the direction perpendicular to the contact interface. Each sub-region includes all atoms of one atomic plane

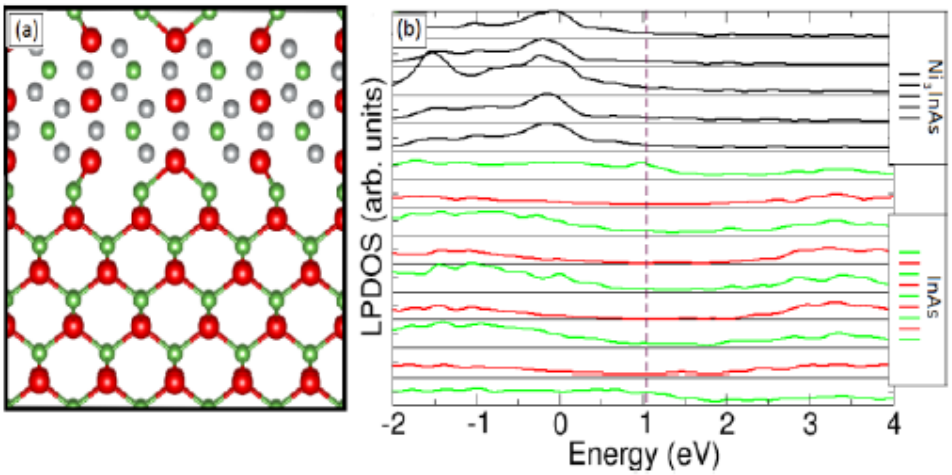


Figure 4.2: (a) The layered projected density of states (LPDOS) for the $Ni_3InAs/InAs$ interface calculated using VASP. (b) Atomic structure for $Ni_3InAs/InAs$ from Ref. [10].

as defined in the $Ni_3InAs/InAs$ system in Fig. 4.2. Then, the LPDOS has been calculated as a convolution of the DOS projected on each atom assigned to the corresponding sub region. As a sequence, the total energy of the system is set to the minimum with respect to the coordinates of all atoms and the cell parameters. Fig. 4.2 shows the geometric structure and density of states projected on atoms of each atomic plane in the $InAs/Ni_3InAs$ (100) heterostructure [6]. Due to the well-known deficiencies of DFT, the LPDOS of InAs does not show a true band-gap. The LPDOS for the in atoms shows a band-gap, which follow the same trend as shown previously for Mo/GaAs [10]. Based upon this, material parameters of the Ni/InAs structure are taken from the Mo/GaAs structure and then scaled appropriately for Ni/InAs [10].

### 4.3.1 Transport Through Contact and Carrier Transport Equations

To study the transport through the contact, we will be solving Poisson and Schrödinger equations self-consistently in 1D and use the finite-difference method with a non-uniform mesh [11]. A real space is divided into individual mesh points ($\psi_i$, $\psi_{i+1}$, and $\psi_{i-1}$). The mesh size regions have a large spaces in the region II and a smaller space in the region I as it shown in Fig. 4.3. A 1D Schrödinger equation in one-electron

approximation can be written as:

$$-\frac{\hbar^2}{2}\frac{d}{dx}(\frac{1}{m^*(x)}\frac{d}{dx})\psi(x) + V(x)\psi(x) = E\psi(x) \tag{4.1}$$

where $E$ is the energy, $\psi(x)$ is the wave function in the $x$-direction, $\hbar$ is a Plank constant divided by $2\pi$, $V$ is the potential energy, and $m^*$ is the carrier effective mass. The Schrödinger equation in a matrix formulation can be written as:

$$H\psi = E\psi \tag{4.2}$$

where $E$ is the energy eigenvalue, and $H$ is a matrix operator of the Hamiltonian representing Schrödinger equation. The matrix operator $H$ can be a real and symmetric depending on the uniform mesh spaces [11]. Poisson equation can be expressed in 1D as:

$$\frac{d}{dx}(\epsilon_s(x)\frac{d}{dx})\phi(x) = \frac{-q[N_D(x) - n(x)]}{\epsilon_0} \tag{4.3}$$

where $\phi$ is the electrostatic potential, $\epsilon_s$ is the dielectric constant, $N_D$ is the ionized donor concentration, and $n(x)$ is the electron density distribution [11]. To obtain the electron distribution in the conduction band profile, we set the electrostatic potential ($V$) to be equal to the conduction band energy [11]. Therefore, the $V$ is correlated to the conduction band energy profile as:

$$V(x) = -q\phi(x) + \Delta E_C(x) \tag{4.4}$$

where $\Delta E_C$ is the energy offset in conduction bands of two materials at the hetero-interface, $q$ is the electron charge, and $V$ is the potential energy in $x$-direction. The electron density $n(x)$ in Eq. (7.3) can be calculated from the wave functions $\psi(x)$ in Eq. (7.1) as follows:

$$n_x = \Sigma_{k=1}^{m}\varphi_k^*(x)\varphi_k(x) \tag{4.5}$$

where $n_x$ is the electron density occupation for each state $k$, and $m$ is the number of bound states at the interface. The electron occupation at each state $k$ can be

described by using Fermi dirac as:

$$n_k = \frac{m^*}{\pi\hbar^2}\int_{E_k}^{\infty} \frac{1}{1+e^{\frac{(E-E_F)}{k_BT}}} dE \tag{4.6}$$

where $E_k$ is the eigen-energy, $E_F$ is Fermi energy level, $k_B$ is the Boltzmann constant and $T$ is the lattice temperature.

### 4.3.2 Solving Schrödinger Equation

To solve Schrödinger equation numerically, we will be considering Eq. (7.1) using a finite difference in a three-point scheme at $x$-direction [11] as shown in Fig. 4.3. The wave function $\psi$ can be approximated into three contributions, $\psi_i$, $\psi_{i+1}$, and $\psi_{i-1}$). We can then write Eq. (7.1) as follows:

$$\frac{-\hbar^2}{2}\left(\frac{2(\psi_{i+1}-\psi_i)}{m_{i+\frac{1}{2}}h_i(h_i+h_{i-1})} - \frac{2(\psi_i-\psi_{i-1})}{m_{i-\frac{1}{2}}h_{i-1}(h_i+h_{i-1})}\right) = E\psi_i \tag{4.7}$$

To solve Schrödinger equation for $\psi_i$, we will consider Hamiltonian matrix $\mathrm{H}_{ij}$ for energy $E$. For each energy, there is an associated wave function $\psi$ taking into account the index grid point mesh $i$ in 1D. Therefore, we can construct the following matrix for Schrödinger equation as:

$$\Sigma_{j=1}^{n} H_{ij}\psi_j = E\psi_j \tag{4.8}$$

where the matrix $H_{ij}$ elements depend on the basis functions $\psi_i$ in the three-point scheme. We can describe the elements as follows:

$$\begin{aligned}
H_{ij} &= -\frac{\hbar^2}{2}\left(\frac{2}{m_i^*+\frac{1}{2}}\frac{1}{h_{i+1}(h_i+h_{i-1})}\right) && \text{if } j = i+1\\
H_{ij} &= -\frac{\hbar^2}{2}\left(\frac{2}{m_i^*-\frac{1}{2}}\frac{1}{h_{i+1}(h_i+h_{i-1})}\right) && \text{if } j = i-1\\
H_{ij} &= -H_{ii} - H_{ii-1} + V_i && \text{if } j = i-1\\
H_{ij} &= 0 && \text{otherwise}
\end{aligned} \tag{4.9}$$

where $i$ is the index which uses to identify the grid points in 1D mesh simulation. The half integer index indicates the point midway between the grid points and $h_i$ is the mesh size between adjacent grid points $x_i$ and $x_{i+1}$. Since the mesh spacing is

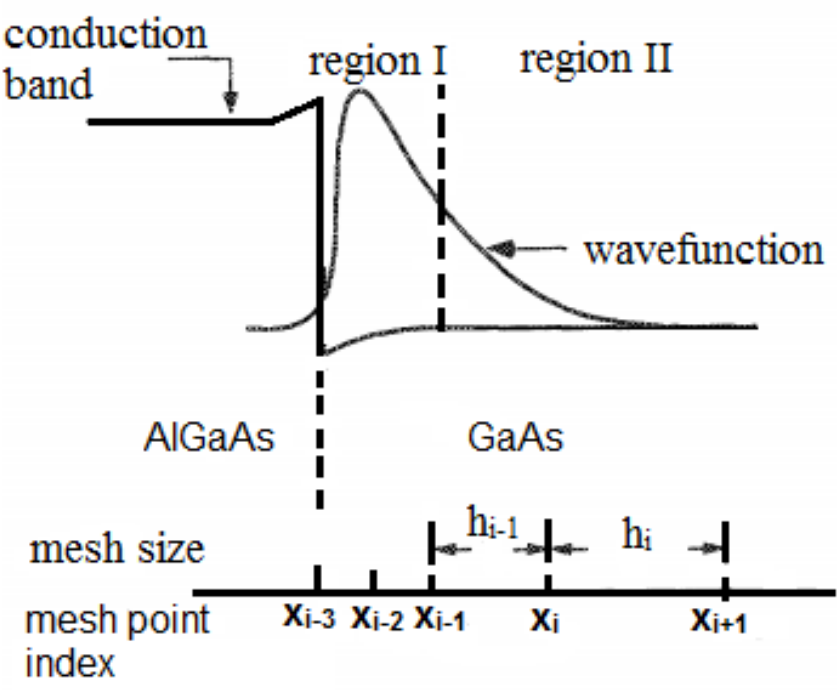


Figure 4.3: Band diagram of the single-heterojunction and the bounded state wave function of GaAs and AlGaAs. The structure shows the discretization of the potential using a non-uniform mesh simulation [11].

a uniform, the matrix $H$ will be a symmetric diagonal matrix (the matrix has non-zero elements) [11]. If the spaces between the mesh are non-uniform, the symmetry matrix $H$ will be destroyed (no matrix elements). However, in the case of the non-uniform mesh, we can define the following parameter $L_i^2$ as:

$$L_i^2 = \frac{(\hbar_i + \hbar_{i-1})}{2} \tag{4.10}$$

were $L$ is a matrix element. By substituting Eq. (4.10) into Eq. (4.9), we will yield the following:

$$\begin{aligned}
H_{ij} &= -\frac{\hbar^2}{2}\left(\frac{1}{m^*_{i+\frac{1}{2}}}\frac{1}{h_i})\frac{1}{L_i^2}\right) \quad \text{if} \quad j = i+1 \\
H_{ij} &= -\frac{\hbar^2}{2}\left(\frac{1}{m^*_{i+\frac{1}{2}}}\frac{1}{h_{i-1}})\frac{1}{L_i^2}\right) \text{if} \quad j = i-1 \\
H_{ij} &= -H_{ii} - H_{ii-1} + V_i \qquad \text{if } j = i \\
H_{ij} &= 0 \qquad \text{otherwise}
\end{aligned} \tag{4.11}$$

If we set $B_{ij} = L_i^2 \, H_{ij}$ then we can obtain the following equation:

$$B = MH \tag{4.12}$$

where $M$ is the diagonal matrix with elements $L_i^2$, and it can be obtained from the FDM. Note that $M = L.L$ and $L$ is a diagonal matrix with $L_i$ elements. Eq. (4.12) suggests that $B$ is a symmetric ($B_{ii+1} = B_{1i}$). Therefore, all the eigenvalues are real and the eigenvectors are orthogonal [11]. This can also provide the transformation matrix that allows to solve for $\psi$ values as follows:

$$B\psi = MH\psi = EM\psi \tag{4.13}$$

where, $H\psi = E\psi$ (Eq. 4.2).
The FDM suggests that the matrix $M$ is a diagonal matrix. Therefore, we can express the the matrix $M$ into the following:

$$M = L.L \tag{4.14}$$

By substituting Eq. (4.14) into Eq. (4.12), we will obtain:

$$B = L.LH \tag{4.15}$$

Therefore, we can re-formulate Eq. (4.13) as follows:

$$L^{-1}BL^{-1}L\psi = L^{-1}LLH\psi = \lambda L^{-1}LL\psi \tag{4.16}$$

or as:

$$H\phi = E\phi \tag{4.17}$$

where

$$H = L^{-1}BL^{-1} \tag{4.18}$$

and

$$\psi = L^{-1}\phi \tag{4.19}$$

Eq. (4.17) can be used to obtain the eigenvalues corresponding to the wave function $\phi$, whereas Eq. (4.19) can be used to obtain the wave function $\psi$ [11]. $\psi$ has two values, ($\psi_k$ and $\psi_l$) which are orthonormal with respect to the matrix $M$ as:

$$\begin{aligned} \psi_k^T M \psi_l &= 1 \quad \text{if } k = 1 \\ \psi_k^T M \psi_l &= 0 \quad \text{if } k \neq 1 \end{aligned} \tag{4.20}$$

### 4.3.3 Solving Poisson Equation

Poisson equation is solved by using the finite-difference method (FDM) and Newton method. This convert the mathematical problem into a system of linear equations via a matrix inversion. The accuracy of the method is therefore directly tied to a finite grid approximation of a continuous system [11]. The Newtons method is a very efficient numerical method for non-linear systems. We will assume that a change in the function $\phi$(x) can be written as $\phi(x) = \phi(x) + \delta\phi(x)$ [11]. By substituting this value into Eq. (4.3), we obtain the equation:

$$\frac{d}{dx}(\epsilon_s \frac{d\phi}{dx}) = \frac{-q[N_D - n(\phi + \delta\phi]}{\epsilon_0} - \frac{d}{dx}(\epsilon_s \frac{d\phi\sigma}{dx}) \tag{4.21}$$

where is $n[\phi + \sigma\phi] = n[\phi] + \sigma n[\phi]$.
The first step in order to apply the FDM is defining the mesh points which create a uniform grid of spatial points. Therefore, Eq. (4.21) can be written as:

$$\begin{aligned} -[\frac{d}{dx}(\epsilon_s \frac{d\phi}{dx})\phi(x) + \frac{q}{\epsilon_0}(N_D - n(\phi))] = \\ \frac{d}{dx}(\epsilon_s \frac{d\phi\sigma}{dx}) - \frac{q}{\epsilon_0}\sigma n[\phi] \end{aligned} \tag{4.22}$$

The term $\phi\sigma n$ is too small and, therefore, $\sigma n[\phi]$ can be written as:

$$\sigma n[\phi] = \ \Sigma_{k=1}^{m}[\sigma(\psi_k^*\psi_k)n_k + (\psi_k^*\psi_k)\sigma n_k \tag{4.23}$$

where

$$\sigma(\psi_k^*\psi_k)n_k = \psi_k^*[\phi+\sigma\phi]\psi_k[\phi+\sigma\phi] - \psi_k^*[\sigma]\psi_k[\sigma] \tag{4.24}$$

and

$$\sigma n_k = n_k(\phi+\sigma\phi) - n_k(\phi) \tag{4.25}$$

By substituting Eq. (4.25) into Eqs. (4.4) and (4.6) for each state $k$, we obtained the equation:

$$\sigma n(\phi) = \Sigma_{K=1}^{M} \frac{m^*}{\pi\hbar^2(1+e^{\frac{(E-Ef)}{KT}})} \times \langle\psi_k|q\sigma\phi|\psi_k\rangle \tag{4.26}$$

The left hand site term is the error in Poisson equation for the function $\phi$ (x). This value can obtained from Eqs. (4.5) and (4.22). To solve the matrix for Poisson equation, we then substitute electron concentration given by Eq. (4.26) into Eq. (4.21) to obtain:

$$-A_i = C_{ii} + \sigma\phi_{i+1} + \sigma\phi_i \left( C_{ii} + \frac{q}{\epsilon_0} \Sigma_{k=1}^{m} \varphi_{k_i}^* \varphi_{k_i} \times \frac{qm^*}{\pi\hbar^2 \left( 1 + e^{\frac{(E-Ef)}{k_BT}} \right)} \right) + C_{ii-1}\delta\phi_{i-1} \tag{4.27}$$

where

$$A_i = \frac{\Sigma_{k=1}^{m} C_{ij} + q(N_{Di} - n_i)}{\epsilon_0} \tag{4.28}$$

The matrix $C_{ij}$ takes the values:

$$\begin{aligned} C_{ij} &= \frac{2\pi_i + \frac{1}{2}}{h_i(h_i + h_{i-1})} && \text{if } j = i+1 \\ C_{ij} &= \frac{2\pi i + \frac{1}{2}}{h_i(h_i + h_{i-1})} && \text{if } j = i-1 \\ C_{ij} &= -C_{ii} - C_{ii-1} && \text{if } j = i \\ C_{ij} &= 0 && \text{otherwise} \end{aligned} \tag{4.29}$$

Eq. (4.29) is set of $n$ error equations with $n$ unknown $\sigma\phi_1$ $\sigma\phi_2$, $\sigma\phi_3$, ..., $\sigma\phi_n$ [11]. This system of equations can be expressed as:

$$C'\sigma\phi = -d \tag{4.30}$$

where is $C'$ is the tri-diagonal non-symmetric matrix, $\sigma\phi$ is the $n\times$ 1 vector which contains electrostatic potential at ech point which has to be added to the former potential profiles, and $d$ is a $n \times 1$ vector including the Poisson errors at each point [11].

### 4.3.4 Self-Consistent Solution of Schrödinger-Poisson Equations

Scheme in Fig. 4.4 illustrates a basic procedure of the solving Schrödinger-Poisson equations self-consistently by iterations of Eqs. (4.1) and (4.3). The eigenvalues $E_k$ obtained from Schrödinger equation can be used to calculate the electron density $n(x)$ using Eq. (4.5). The calculated $n(x)$ and the given donor concentration $N_D(x)$ are used to calculate $\phi$ $(x)$ via Eq. (4.3). The new potential energy $V(x)$ is then obtained from Eq. (4.4). The subsequent iteration will yield the final self-consistent solutions for $V(x)$ and $n(x)$.

## 4.4 Material Parameters

### 4.4.1 Band Gap Energy

In order to gain the physical insight into carrier transport through the contact, we have employed DFT calculations taken from previous study on NiInAs, InAs,

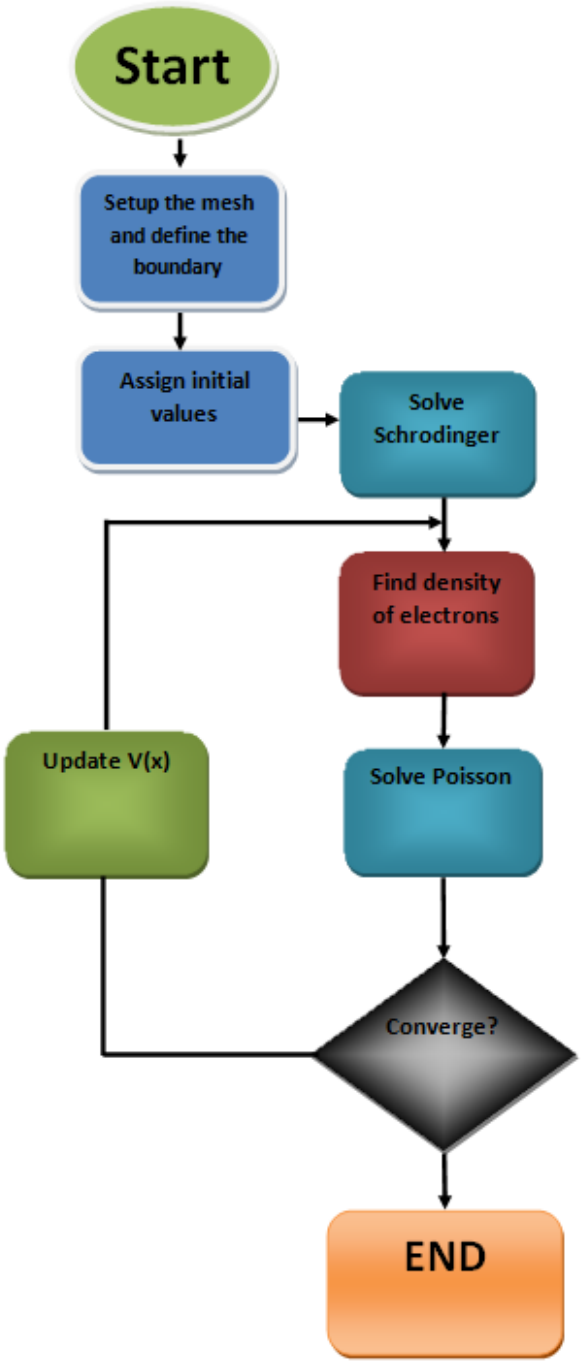


Figure 4.4: Flowchart shows the approach of solving the Schrödinger-Poisson system self-consistently in an iterative process.

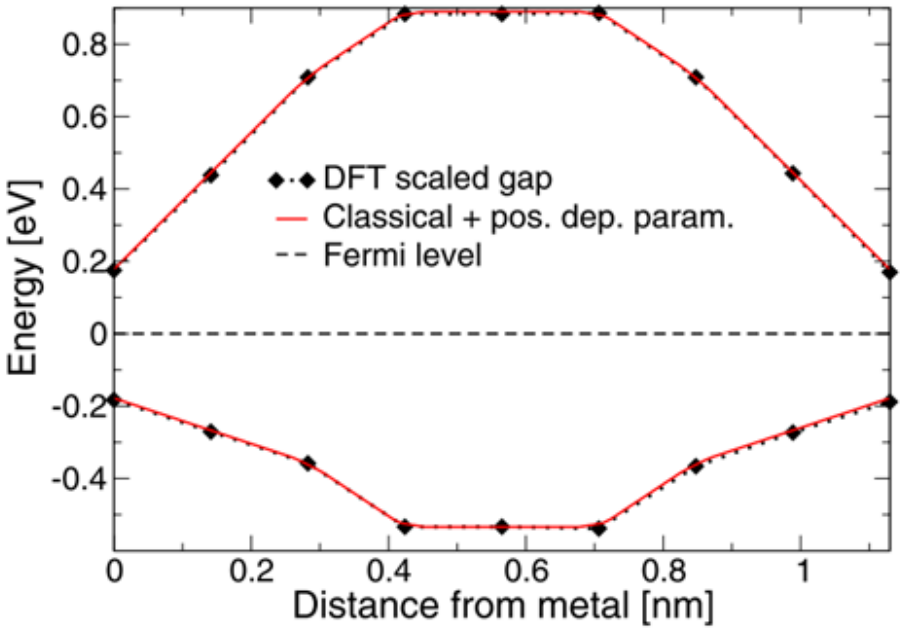


Figure 4.5: Conduction and valence band edges as a function of the position (continuous red line) and extracted from the DFT calculations (black diamonds) of GaAs. Fermi level (dashed black line) is set at 0 eV [10].

AlAsSb [12, 6, 13]. Due to the well-known difficulty with the inclusion of many-body Coulomb interactions (exchange and correlations) in a DFT, the LPDOS of InAs does not reproduce a true band gap. However, the LPDOS for the $Ni_3InAs/InAs$ atoms has a band gap which follows the same trend as seen previously for the Mo/GaAs [10].

The DFT calculations allows us to extract energy position of the conduction and valence bands in a semiconductor with respect to a metal which depends on the real-space position of Mo/GaAs as shown in Fig. 4.5 [10]. InAs is well known as a direct band gap material and the calculation gives a direct band gap of 0.35 eV which coincides with experimental values that have been reported [12].

The energy band gap of $AlAs_{0.47}Sb_{0.53}$ has been calculated by use Vegards law using Eq. (7.31) which assumes both components $A$ material and $B$ material having the same crystal structure at the same temperature [13]. $E_g^{AB}$ is the energy band gap of binary alloys $A$ and $B$ (which are AlAs and AlSb in our simulations) as shown in Fig. 4.6. The parameter $x$ is the concentration of material $A$ in the $AB$ composition and $C$ is the bowing parameter accounting for the deviation from a linear interpolation (the virtual crystal approximation) between the two alloys [13]. Then the Vegard

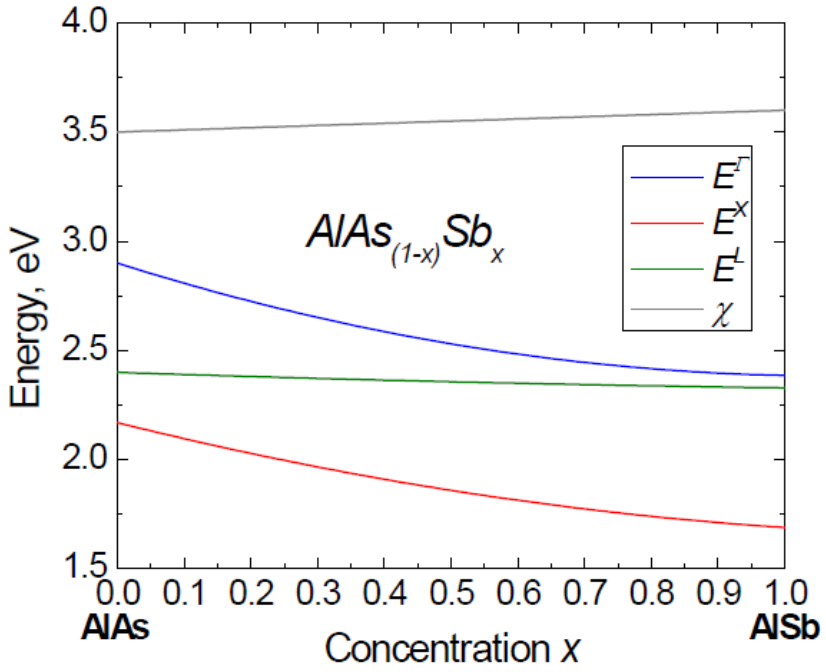


Figure 4.6: Band gaps $E_g^{\Gamma}$, $E_g^x$, $E_g^L$ and electron affinity $\chi$ on the composition $x$ [13].

law for $AlAs_{0.47}Sb_{0.53}$ with the component ($x = 0.47$) can be written as:

$$E_g^{AB} = x.E_g^A + (1-x)E_g^B - x.(1-x).C \tag{4.31}$$

The values of AlAs, $E_g = 2.17$ eV and AlSb $E_g = 1.69$, $C = 0.28$, $x = 0.47$ and $(1-x) = 0.53$ have been extracted from Fig. 4.7 based on results reported in Ref. 14 [13], Table 4.1. By substituting these values in Eq. (4.31), we have calculated the energy band gap of $AlAs_{0.47}Sb_{0.53}$ as 1.846 eV.

Table 4.1: Energy band parameters: InAs, AlAs, AlSb and $AlAs_{0.47}Sb_{0.53}$.

| Parameters | InAs Ref. [14] | AlAs Ref. [14] | AlSb Ref. [15] | C AlAsSb [14, 15] |
|---|---|---|---|---|
| $E_g^{\Gamma}$ | 0.354 | 2.9 | 2.386 | 0.45 |
| $E_g^x$ | 1.374 | 2.17 | 1.69 | 0.28 |
| $E_g^L$ | 1.084 | 2.4 | 2.329 | 0.03 |
| $\Delta_{so}$ | 0.39 | 0.28 | 0.676 | 0.15 |
| $\chi$ | 4.9 | 3.5 | 3.6 [16] | 0 |
| $a, \mathring{A}$ | 6.058 | 5.661 | 6.135 | |

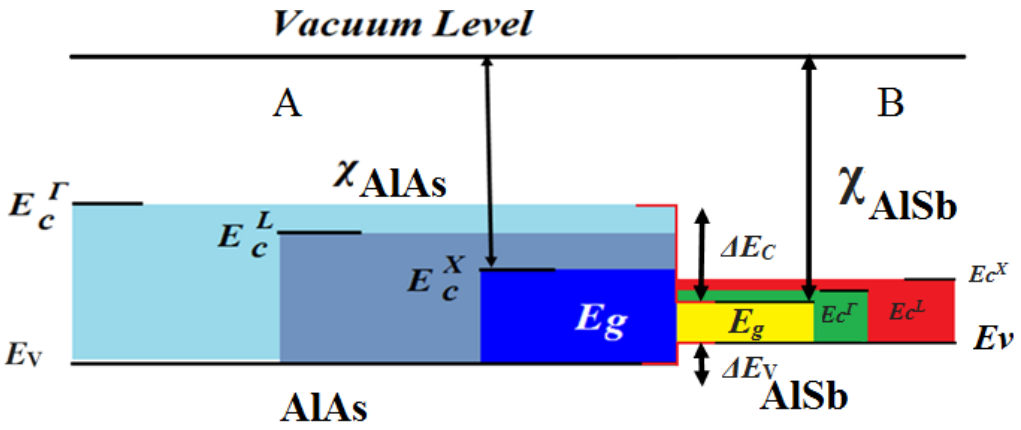


Figure 4.7: The schematic showing the energy band gap diagram between AlAs and AlSb.

### 4.4.2 Band Gap Offset

The alignment of the energy bands at a heterojunction is called band gap offset as shown in Fig. 4.7 [17]. To calculate the band gap offset, we will be using Anderson rule. The rule can be used for the energy band diagrams construction of the heterojunction between two semiconductor materials for III-V semiconductors [18]. The conduction band offset rule states that the vacuum level of two semiconductors in a heterostructure should be aligned. Energy band diagram can be constructed with respect to the vacuum level using the electron affinity $\chi$ and the band gap $E_g$ for each semiconductor [19]. Consider our two alloys of InAs and GaAs (used as a reference material in the simulations) as shown in Fig. 4.8, we can calculate electron affinity of InAs. $\triangle E_c$ can write:

$$\triangle E_c = \chi(InAs) - \chi(GaAs) \tag{4.32}$$

where $InAs$ is the semiconductor 1 and $GaAs$ is the semiconductor 2. The conduction bands of GaAs and InAs as are shown in Fig. 4.8. Similarly we can calculated the band gap offset of AlAsSb as it shows in Table 4.2. This equation can be also used to calculate the valence band offset [18].

### 4.4.3 Effective Mass

Kane theory has been used to calculate effective masses $m^*$ at the bottom of the conduction band. The formula correlates effective mass to an energy band gap $E_g$ [13]. From Kane formula the electron effective mass for III-V semiconductor can

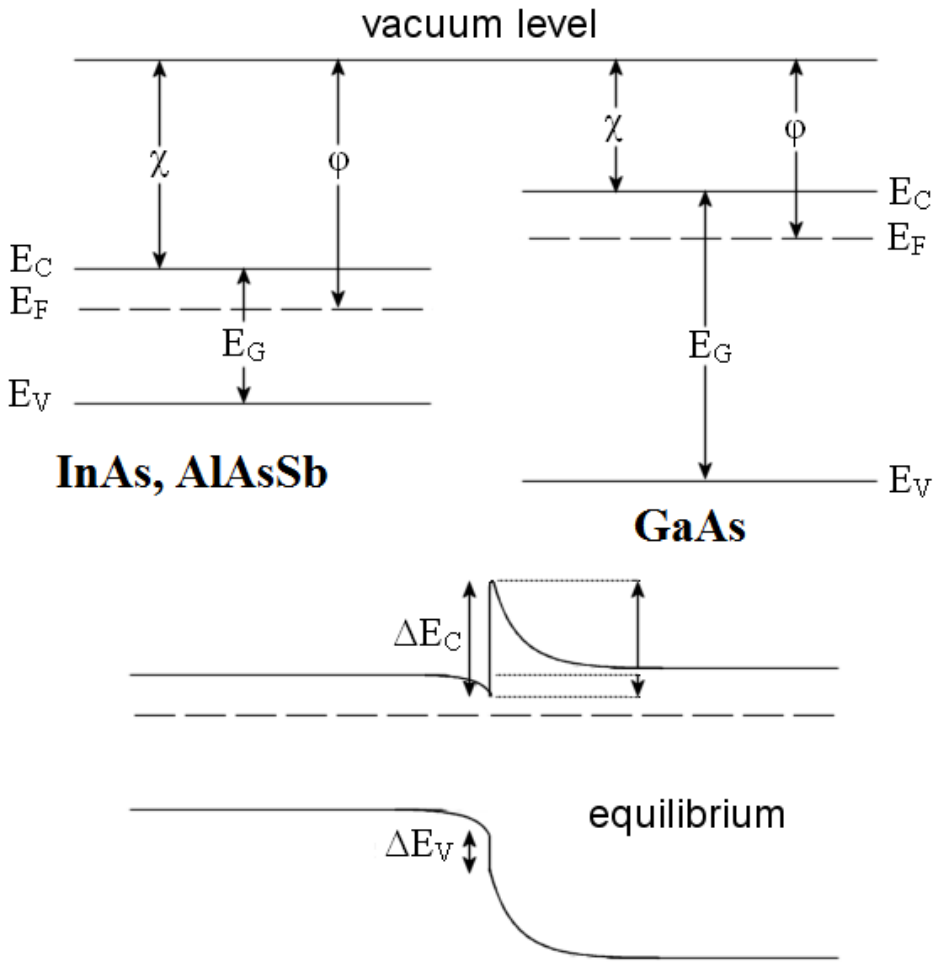


Figure 4.8: Band diagrams for the heterojunction by Anderson's rule. The junction alignment at equilibrium (bottom) is predicted based on flat vacuum alignment (top).

be expressed as:

$$\frac{m^*}{m_0} = [1 + P^2.\frac{1}{3}\frac{2}{3E_g} + \frac{1}{3E_g + \Delta_{so}}]^{-1} \tag{4.33}$$

where $E_g$ is the energy band gap, and $\Delta_{so}$ is the compound spin-orbit splitting energies calculated from the Eq. (4.31) as it reported in Table 4.1, $m_0$ is the mass of the electron and $P$ is the momentum matrix element uses in the Kane Hamiltonian. The momentum matrix element can obtain from the lattice constant of the material as follow:

$$P = \sqrt{\frac{3\Pi}{a^2}} \tag{4.34}$$

where $\Pi = 641$ eV. $A^2$ is a Kane parameter [13], $a$ is the lattice constant. The lattice constant for ternary alloy can be calculated using Vegard approximation which assumes a linear relation between the crystal lattice parameter of the alloy and the concentration $x$ of the two constituent compounds ($a$ and $B$) as follows:

$$a_{AB} = xa_A + (1 - x).a_B \tag{4.35}$$

where is a is a crystal lattice parameter of an alloy and the concentrations of the constituent compounds. Table 4.2 and Fig. 4.9 show the effective masses $m_*$ and the crystal lattice parameters for the compounds InAs, AlAs, GaAs and AlSb for a concentration $x$ at $\Gamma$-point [13]. With the use of Eqs. (4.33), (4.34) and (4.35), we calculate the effective mass $m_*$ of $AlAs_{0.47}Sb_{0.53}$, and InAs to be 0.088 $m_0$ and 0.23 $m_0$, for the direct energy gap at $\Gamma$- point respectively.

Table 4.2: InAs, $Ni_3InAs$ and $AlAs_{0.47}Sb_{0.53}$ material and structure parameters from literature used in a modelling of the Al $As_{0.47}Sb_{0.53}$ contact, electron mobility has been obtained from Monte-Carlo simulation as it shows in Fig. 4.10.

| Surface | Thickness [nm] | $n$-type doping [$cm^{-3}$] | $p$-type doping [$cm^{-3}$] | $E_g$ [eV] | $\Delta E_C$ [eV] | $\mu$ [$cm^2$/Vs] | $m_e$ [$m_0$] | $\varepsilon_r[\varepsilon_0]$ |
|---|---|---|---|---|---|---|---|---|
| InAs | 8.5 | $3\times 10^{19}$ | $1\times 10^{14}$ | 0.354 | -0.71 | 200 | 0.023 | 15.50 |
| InAs | 2.5 | $1\times 10^{16}$ | $1\times 10^{14}$ | 0.354 | -0.71 | 1960 | 0.023 | 15.50 |
| Al $As_{0.47}Sb_{0.53}$ | 960 | $1\times 10^{14}$ | $1\times 10^{16}$ | 1.846 | 0.315 | 1350 | 0.088 | 10.95 |

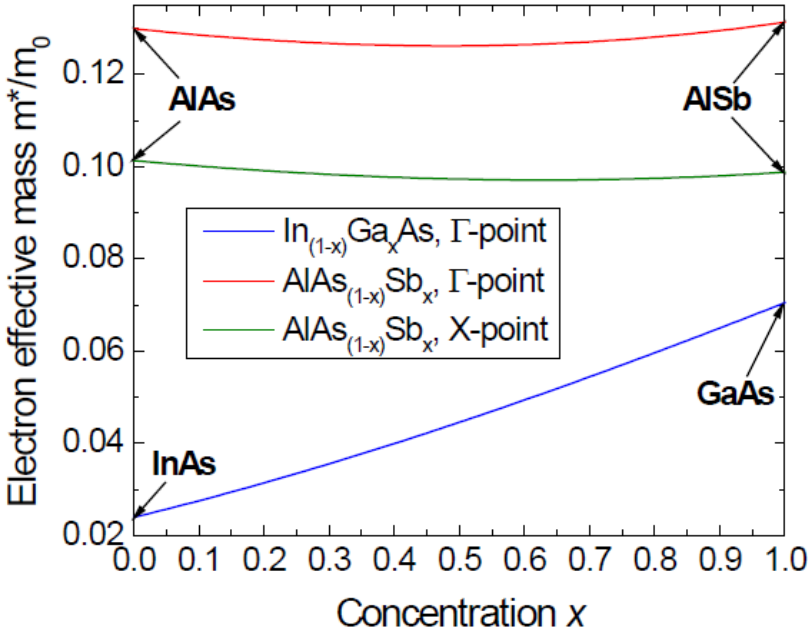


Figure 4.9: The computed dependences of electron effective masses m* on the concentration x for $AlAs_{0.47}Sb_{0.53}$ alloys [13].

## 4.5 Schottky Barrier Hight and Metal Work Function

Schottky barrier hight (SBH) is a potential barrier between metal and semiconductor and can be also defined as the potential difference between Fermi energy of the metal and the band edge [15] as we discussed earlier in Chapter 2. This barrier can also be defined from the relation between metal work function and electron affinity as follows:

$$q\phi_{SH} = q(\phi_M - \chi) \tag{4.36}$$

where $\phi_{SH}$ is Schottky barrier, $\phi_M$ is the work function, $\chi$ is the electron affinity and $q$ is the charge of electron. If we assume a bulk metal work function of Ni to be 5.01 eV and electron affinity reported in Ref. [6], the SBH will be 0.3 eV. The SBH takes the value of 0.11 eV when the work function decreases to 4.79 eV. Eq. (4.34) and Table 4.3 show the extracted SBH for a different range of work functions. Note that the metal work functions have been taken from previous study by different groups [6, 20].

Table 4.3: Sheet resistance of nanoscale metal contact for several combination of parameters.

| Affinity/Band gap | Effective mass | Schottky barrier height [eV] | Sheet Resistance [Ω/sq] |
|---|---|---|---|
| Constant | Constant | 0.11 | 165 |
| Constant | Constant | 0.30 | 203.7 |
| Narrowing | Position dependent | 0.11 | 63.85 |
| Narrowing | Position dependent | 0.30 | 90.9 |

## 4.6 Electron Mobility

In order to determine the mobility of InAs used in the simulations, we estimate the electric field first, assuming 1 V bias applied across the contact [5]. Electric field $F$ can be calculated as $F = v/t$ where $t$ is the thickness of the structure (11 nm InAs and 960 nm $AlAs_{0.47}Sb_{0.53}$) as:

$$F = \frac{V}{t(InAs + AlAsSb)} = \frac{1V}{961nm} = 10kV/cm \tag{4.38}$$

The electron mobility in InAs (intrinsic) plotted in Fig. 4.10 as a function of applied electric field has been obtained from bulk ensemble Monte Carlo simulations [5]. Details of these Monte Carlo simulations can be found in Ref. [5]. Fig. 4.10. shows that, at an electric field of 10 kV/cm, the intrinsic electron mobility of $n$-type InAs doped to $3\times10^{19}cm^{-3}$ (nearly intrinsic) is 1960 $cm^2$/Vs, and 200 $cm^2$/Vs when $n$-type doped to $3\times10^{19}cm^{-3}$ [21] as collected in Table 4.2. Finally, the electron mobility of $p$-type $AlAs_{0.47}Sb_{0.53}$ (doping concentration $1\times$ $10^{16}cm^{-3}$) used in the 1DPS is 1350 $cm^2$/Vs and is based on the experimental data taking into consideration the material composition of $AlAs_{0.47}Sb_{0.53}$ and carrier concentration.

## 4.7 1D Transport Simulations

A source-drain (S-D) contact model used in the simulations was chosen to match the size and the composition of the experimental structure made of an 11 nm thick InAs channel deposited on $p$-type $AlAs_{0.47}Sb_{0.53}$ buffer (doped to $1\times10^{16}cm^{-3}$). Then the Ni is deposited as a metal contact at the S-D followed by a thermal treatment to create an 8.5 nm thick $Ni_3InAs$ alloy, leaving only 2.5 nm thickness of un-doped InAs layers acting as a channel as shown in Fig. 4.1.

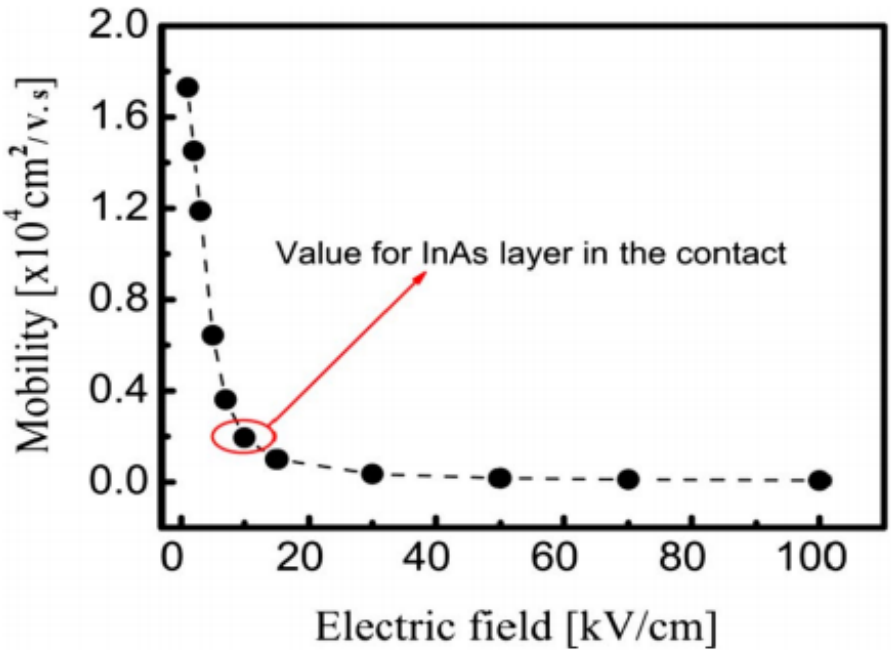


Figure 4.10: Electron mobility vs. applied electric field in bulk InAs obtained from ensemble Monte Carlo simulations [21].

Fig. 4.11 (a and b) shows the conduction band, valence bands and Fermi level overlapped with electron density from the 1DPS solutions. We assume a bulk metal work function of Ni to be 5.01 eV and calculate the SBH as a potential difference between the work function and the electron affinity. For the metal work function of 5.01 eV and affinity of 4.9 eV [6], the SBH was extracted to be 0.11 eV and an electron sheet resistance will be 165 Ω/sq. When the metal work function takes a value of 4.79 eV [6], the SBH increases from 0.11 eV to 0.30 eV. Due to the increase in the SBH, a sheet resistance increases to 203.7 Ω/sq. This value is approximately around 110 % larger than the experimentally measured one because electrons have to tunnel through a larger potential barrier [4]. In a comparison, the sheet resistance at a metal work function of 5.01 eV is larger by about 70 % than the experimentally observed.

## 4.8 Band Gap Narrowing

The band gap narrowing in InAs semiconductor is modelled as follows. The coordinates for the band gap narrowing in InAs layer are obtained from DFT calculations [8] of a nanoscale Mo/GaAs contact assuming that the same narrowing

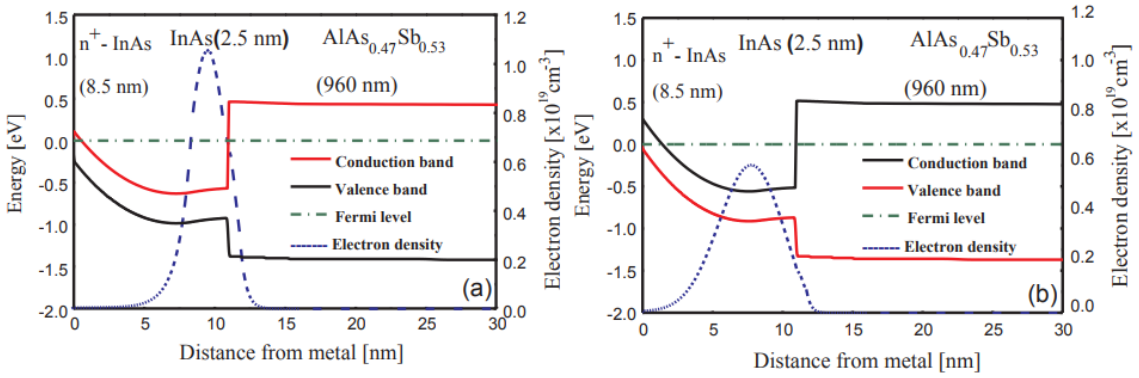


Figure 4.11: Conduction and valence band profiles at equilibrium of the InAs (8.5 nm)/ InAs (2.5 nm)/$AlAs_{0.47}Sb_{0.53}$ heterostructure assuming a constant band gap at the interface for Schottky barrier height of (a) 0.11 eV and (b) 0.30 eV.

occurs in the band gap of InAs of the Ni/InAs contact. The region of InAs at the metal-semiconductor interface is divided into 5 equal regions. For every node of the 1D mesh simulation, we compute the distance to the metal contact and adjust the values of InAs (electron effective mass, the band gap and the electron affinity) using the calculated position dependent values [8] as shown in the caption of Fig. 4.12 (a).

Fig. 4.12 (a and b) shows conduction and valence bands overlapped with electron density due to the effect of band gap narrowing for two values of Schottky barrier height (0.1 eV and 0.3 eV). The electron wave function penetration is substantially reduced here due to a change in the shape of Schottky barrier which becomes thinner for electrons to tunnel through. As a result, an electron sheet resistance has decreased from 90.9 Ω/sq to 63.85 Ω/sq (by about 42 %).

## 4.9 Source-Drain Series Resistance

Fig. 4.13 shows the variation in a sheet resistance with a metal work function obtained from 1DPS simulations assuming a constant band gap (band gap without narrowing) in the InAs layer (black circles) and assuming the band gap narrowing (red square). Only when the band gap narrowing is taken into account, the simulations give an agreement with the experimental value (green diamond). Hence, with the band gap narrowing, our results give an electron sheet resistance $R_{sh}$ of 90.9 Ω/sq, which is in a good agreement with the measured result of 97 Ω/sq [3].

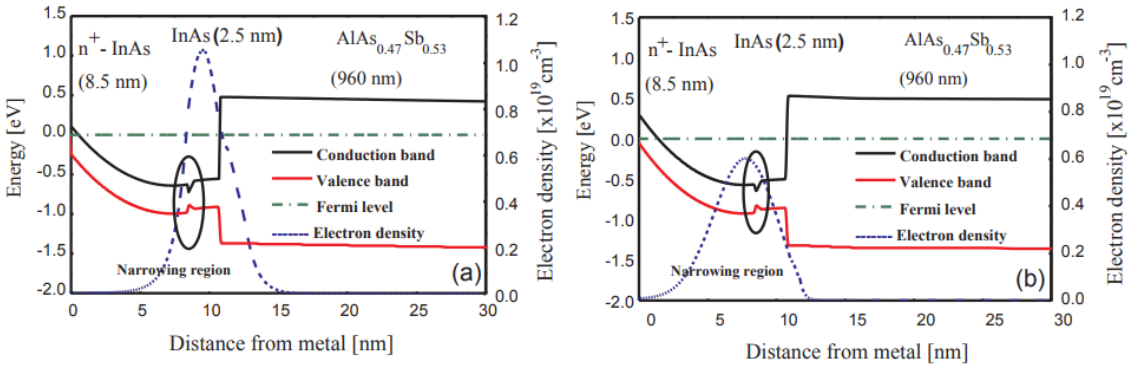


Figure 4.12: (a) Conduction and valence band profiles for Ni/InAs (8.5 nm)/InAs (2.5 nm)/$AlAs_{0.47}Sb_{0.53}$ (960 nm) heterostructure assuming the band gap narrowing and a SBH of 0.11 eV at equilibrium. The energies for the band gap narrowing of InAs at the interface from the DFT are: $\Delta E_G$ (0.2 nm) = 0.354 eV, $\Delta E_G$ (0.4 nm) = 0.204 eV, $\Delta E_G$ (0.6 nm) = 0.254 eV, $\Delta$ E $_G$ (0.8 nm) = 0.304 eV, $\Delta E_G$ (1.0 nm) = 0.354 eV. (b) The constant band gap for a SBH of 0.30 eV. The band gap narrowing of InAs at the interface follows the same steps as in (a).

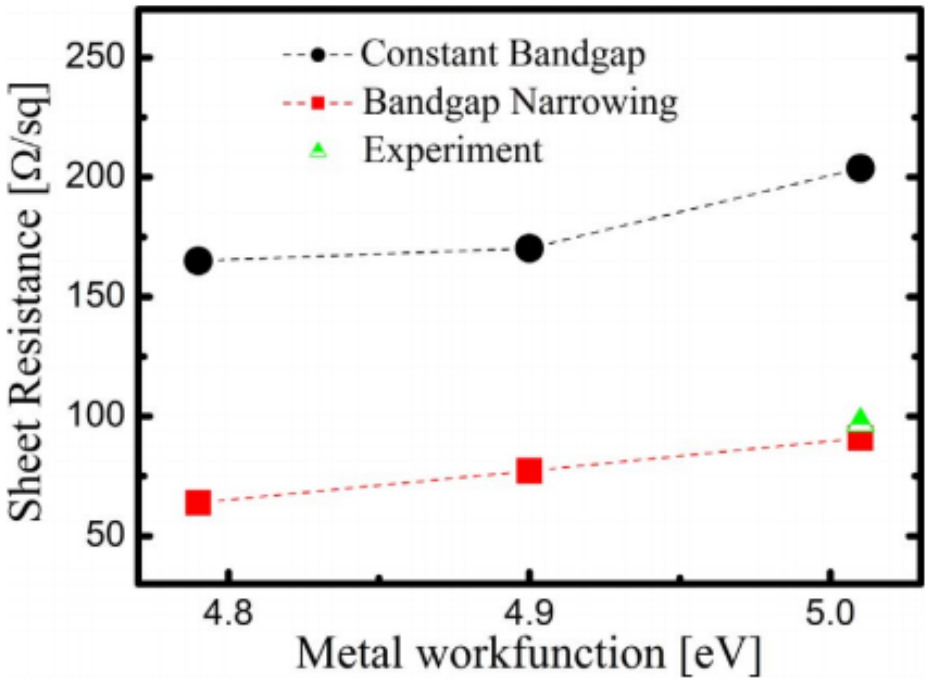


Figure 4.13: Sheet resistance for InAs (8.5 nm)/InAs (2.5 nm)/$AlAs_{0.47}Sb_{0.53}$ (960 nm) contact heterostructure as a function of metal work function (Ni) comparing simulations using the same band gap in whole InAs and with those when the band gap narrowing towards metal-semiconductor interface is accounted for. The experimental value of sheet resistance [3] is shown by green triangle.

If the band gap narrowing is not included, the abrupt metal semiconductor interface results in a lower tunnelling probability which increases the electron sheet resistance to 203.7 Ω/sq. The results obtained for different combinations are collected in Table 4.3. When we take into account the band gap narrowing, the sheet resistance decreases. This is caused by the dependence of the tunnelling (a penetration of electron wave function though a barrier) probability on the barrier shape. Notably thes barrier becomes narrower which leads to an increase in the current flow through the contact [22].

## 4.10 Conclusion

We have developed a multi-scale model for electron transport in metal- semiconductor contacts using first principle calculations (DFT) which provide input for the 1D self-consistent PS simulations. We have demonstrated that the transport properties, in particular, the electron sheet resistance gives a better agreement with experimental observations when taking into account the band gap narrowing in the InAs at the interface than when using a method of SBH and constant semiconductor band gap and affinity. We have thus shown that the inclusion of a realistic band structure at the interface results in a larger tunnelling current than would have been obtained from Schottky contact model while assuming a bulk work function of Ni (5.01 eV). This decreases the sheet resistance of the contact to 90.9 Ω/sq which is in a very good agreement with the experimentally measured value of 97 Ω sq [3]. This agreement reveals that the band gap narrowing plays an essential role in determination of the sheet resistance of a nano-scale metal contact.

# References


[1] S. Adachi. *Properties of semiconductor alloys: group IV, III-V and II-VI semiconductors*. Vol. 28. John Wiley and Sons, 2009 (cit. on pp. 65, 67).

[2] K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen, H. S. Kim, C. Liu, Y. Chueh, and E. Plis. "Quantum confinement effects in nanoscale thickness InAs membranes". In: *Nano letters* 11.11 (2011), pp. 5008–5012 (cit. on p. 65).

[3] R. Oxland, S. Chang, X. Li, S. Wang, G. Radhakrishnan, W. Priyantha, M. J. H. Van Dal, C. H. Hsieh, G. Vellianitis, and G. Doornbos. "An ultralow resistance ultrashallow metallic source/drain contact scheme for III–V NMOS". In: *Electron Device Letters* 33.4 (2012), pp. 501–503 (cit. on pp. 65–67, 85–87).

[4] S. E. Mohney, Y. Wang, M. A. Cabassi, K. K. Lew, S. Dey, J. Redwing, and T. S. Mayer. "Measuring the specific contact resistance of contacts to semiconductor nanowires". In: *Solid State Electronics* 49.2 (2005), pp. 227–232 (cit. on pp. 66, 84).

[5] K. Kalna, N. Seoane, A. J. Garcia-Loureiro, I. G Thayne, and A. Asenov. "Benchmarking of scaled InGaAs implant-free nanoMOSFETs". In: *Transactions on Electron Devices* 55.9 (2008), pp. 2297–2306 (cit. on pp. 66, 83).

[6] G. Schusteritsch, S. P. Hepplestone, and C. J. Pickard. "First principles structure determination of interface materials: The $Ni_x$InAs nickelides". In: *Physical Review B* 92.5 (2015), p. 054105 (cit. on pp. 67, 68, 77, 82, 84).

[7] A. Pacelli. "Self-consistent solution of the Schrödinger equation in semiconductor devices by implicit iteration". In: *Transactions on Electron Devices* 44.7 (1997), pp. 1169–1171 (cit. on p. 67).

[8] J. P. Perdew, K. Burke, and M. Ernzerhof. "Generalized gradient approximation made simple". In: *Physical Review Letters* 77.18 (1996), p. 3865 (cit. on pp. 67, 84, 85).

[9] M. Ameri, B. Fatima, A. Touia, M. Faudil, D. Hachemane, K. Boudia, A. Slamani, and A. Aze-Eddine. "Ab Initio Calculations Study of Structural and Electronic Properties of Ternary Alloy $Al_xIn_{1-x}As$". In: *Materials Sciences and Applications* 3.10 (2012), p. 674 (cit. on p. 67).

[10] M. Aldegunde, S. P. Hepplestone, P. V. Sushko, and K. Kalna. "Multi scale simulations of a Mo/$n^{+-}$GaAs Schottky contact for nano scale III-V MOSFETs". In: *Semiconductor Science and Technology* 29.5 (2014), p. 054003 (cit. on pp. 67, 68, 77).

[11] I. H. Tan, G. L. Snider, L. D. Chang, and E. L. Hu. "A self consistent solution of Schrödinger Poisson equations using a nonuniform mesh". In: *Journal of Applied Physics* 68.8 (1990), pp. 4071–4076 (cit. on pp. 68–73, 75).

[12] E. K. U. Gross and R. M. Dreizler. *Density functional theory*. Vol. 337. Springer, 2013 (cit. on p. 77).

[13] Y. Fedoryshyn. "Modeling, growth and characterization of InGaAs/AlAsSb quantum well structures for all-optical switching based on intersubband transitions". PhD thesis. Lviv Polytechnic National University, 2012 (cit. on pp. 77–79, 81, 82).

[14] M. S. Shur. *Handbook Series on Semiconductor Parameters*. Vol. 1. World Scientific, 1996 (cit. on p. 78).

[15] I. Vurgaftman, J. R Meyer, and L. R. Ram-Mohan. "Band parameters for III–V compound semiconductors and their alloys". In: *Journal of Applied Physics* 89.11 (2001), pp. 5815–5875 (cit. on pp. 78, 82).

[16] T. E. Fischer. "Reflectivity, photoelectric emission, and work function of AlSb". In: *Physical Review* 139.4A (1965), A1228 (cit. on p. 78).

[17] J. P. Heida, B. J. Van Wees, J. J. Kuipers, T. M. Klapwijk, and G. Borghs. "Spin-orbit interaction in a two-dimensional electron gas in a InAs/AlSb quantum well with gate-controlled electron density". In: *Physical Review: B* 57.19 (1998), p. 11911 (cit. on p. 79).

[18] R. L. Anderson. "Experiments on ge gaas heterojunctions". In: *Solid State Electronics* 5.5 (1962), pp. 341–344 (cit. on p. 79).

[19] E. O. Kane. "Band structure of indium antimonide". In: *Journal of Physics and Chemistry of Solids* 1.4 (1957), pp. 249–261 (cit. on p. 79).

[20] J. L. Freeouf and J. M. Wood. "Schottky barriers: An effective work function model". In: *Electronic Structure of Metal-Semiconductor Contacts*. Springer, 1990, pp. 154–156 (cit. on p. 82).

[21] B. Benbakhti, A. Martinez, K. Kalna, G. E. Hellings, K. D. Meyer, and M. Meuris. "Simulation Study of Performance for a 20-nm Gate Length $In_{0.53}Ga_{0.47}As$ Implant Free Quantum Well MOSFET". In: *Transactions on Nanotechnology* 11.4 (2012), pp. 808–817 (cit. on pp. 83, 84).

[22] A. H. Mohamed, R. Oxland, M. Aldegund, S. P. Hepplestone, P. V. Sushko, and K. Kalna. "Narrowing of band gap at source/drain contact scheme of nanoscale InAs-nMOS". In: *Solid State Electronics* 49.2 (2018), pp. 227–232 (cit. on p. 87).

# Chapter 5

# Top-Down Fabrication of ZnO Devices, Characterisation Results, Analysis and Discussion

## 5.1 Introduction

In this chapter, a top down fabrication approach used to fabricate zinc oxide field-effect transistors (ZnO NW-FETs) and Zinc Oxide thin-film transistors (ZnO TFTs) will be discussed. The devices have been fabricated at Southampton Nanotechnology Centre which provides state of the art facilities for design and fabrication of semiconductor devices [1]. ZnO TFTs has been fabricated by using a top-down fabrication method on thermally oxidized Si via remote plasma atomic layer deposition (PEALD) for different channel length ($L_{\mathrm{ch}} = 10\ \mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m) [2]. The process starts of by ZnO deposited over a $SiO_2$ pillar first and aniso-tropically dry etched by aniso-tropically reactive ion etch (RIE) to produce ZnO NWs as shown in Fig. 5.1(a). This top-down fabrication approach with a low temperature film deposition is promising technology for future low-cost mass manufacturable sensors for health care and biomedical research [2]. The electrical characterisation is carried out by using four probes measurement to study the impact of channel length of $L_{ch}$ scaling on electrical characteristics of ZnO TFTs. We will also be investigating the behaviour of breakdown voltage and sub-threshold voltage for each channel length. A transmission line method (TLM) used to calculate the contact resistance ($R_C$), and effective ($L_{\mathrm{eff}}$) and channel ($L_{\mathrm{ch}}$) electron mobility is also discussed in

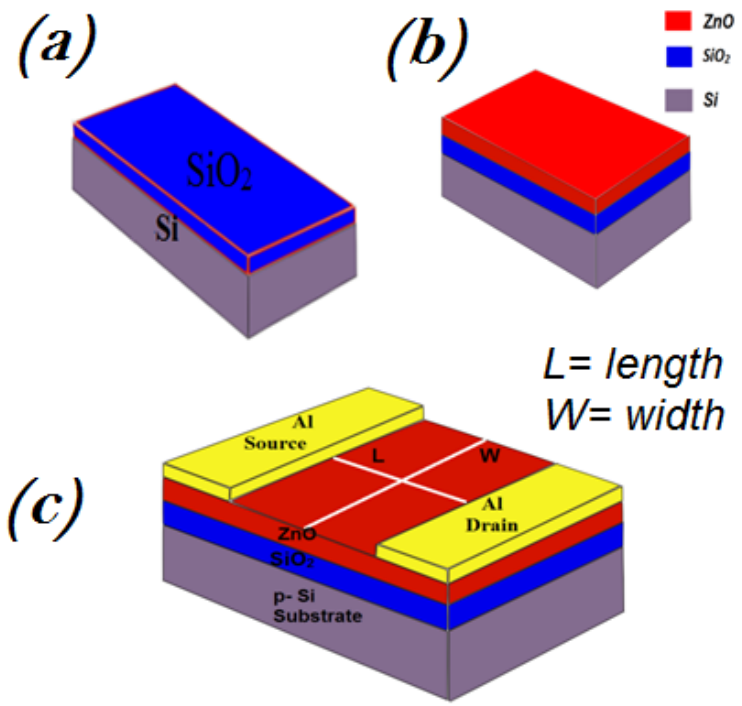


Figure 5.1: Top-down fabrication process of ZnO TFTs (a) $SiO_2$ thermally grown through wet oxidation 200 nm and $SiO_2$ dry thermal oxidation in the RIE to form a trench. (b) ZnO thin film deposited by the remote plasma. (c) Schematic structure of ZnO thin-film FET fabricated by using top-down fabrication method via remote plasma atomic layer deposition (ALD).

this chapter. The electron channel mobility has been obtained from the expression for the drain current of MOSFET in a linear regime using a MOSFET basic theory at room temperature [2]. In addition, we will be studding the fabrication of ZnO NWs field-effect transistors (NWs-FETs) using a top-down fabrication method from Southampton Nanotechnology Centre. The top-down fabrication method starts with a thin film deposition by remote plasma enhanced-ALD (PEALD). The PEALD is followed by aniso-tropically reactive ion etch (RIE) to produce ZnO NWs with different channel lengths ($L_{\mathrm{ch}}$ = 20 $\mu$m, 10 $\mu$m, and 2 $\mu$m). The optical and electrical characterisations is then carried out to study the impact of scaling down channel length ($L_{\mathrm{ch}}$) in the transistors. Finally, the chapter will be concluded with a comprehensive summary.

## 5.2 ZnO TFTs Fabrication

### 5.2.1 Remote Plasma Enhanced Atomic Layer Deposition

The atomic layer deposition (ALD) of ZnO is a process, that has shown a great potential to deposit a conformal and high quality film [2]. Plasma assisted ALD has been wide used, and it has been reported that, the uses of plasma is reduced the (OH) impurity, as a result, that improve the conductivity of semiconductor thin-film and reduce defects in dielectric materials [2]. PEALD has widely demonstrated a high quality dielectric films, such as for high-k dielectric materials [2]. The technique is cyclic, based on two self-limiting reactions, metallization and oxidation. These reactions are separately executed on a substrate surface. In what follows, we describe in detail the fabrication process used for ZnO TFTs. Diethyl Zinc (DEZ) is used as the Zn metal precursor. During metallization, DEZ adsorbs to a substrate surface [2]. Subsequently, the absorbed DEZ reacts with an oxidant in the oxidation step. Usually, the oxidant is water which is widely known as thermal ALD [2]. To assure both reactions are executed separately, pump and purge steps are implemented between the metallization and oxidation steps. In each ALD cycle, the surface is left with one mono-layer of ZnO [2]. The ALD process of ZnO using water as an oxidant has already been extensively studied and can be considered as a model system for ALD. ZnO films were prepared on a 200 nm $SiO_2$/$p$-Si substrate. The Si wafers with a 200 nm thick thermally grown $SiO_2$ were cleaned in acetone and Iso-propyl alcohol (IPA) ultrasonically for 1 min. The samples were immediately loaded into the reactor and ALD process was performed based on a design [2].

### 5.2.2 Top-Down Fabrication of ZnO TFTs

With the optimized remote PEALD conditions we discussed previously, a top-down ZnO TFTs were fabricated using mature >1 $\mu$m photo-lithography and anisotropic reactive ion etching (RIE) to produce TFTs [2]. Fig. 5.1(a) shows the fabrication process steps. The process starts with a $p$-type Si wafer. The wafer was cleaned in fuming nitric acid for 15 minutes and dipped in a hydrofluoric acid before a layer of $SiO_2$ was thermally grown by dry thermal oxidation [2]. The $SiO_2$ was then etched aniso-tropically by photo-lithography pattern transfer and reactive ion

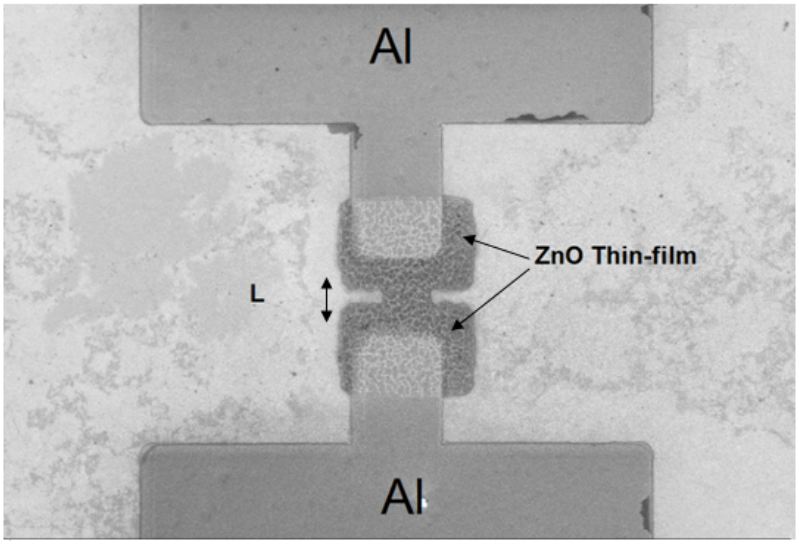


Figure 5.2: SEM images of ZnO TFTs with the Al pad which serves as contacts.

etching (RIE). The $SiO_2$ etch was executed in $CHF_3$, and Ar mixture at a pressure of 30 mTorr [2]. Fig. 5.1(b) shows the $SiO_2$ trench formed after the RIE etch. A 35 nm layer of ZnO film was deposited on top of the trenches seen in Fig. 5.1(b). The ZnO film was deposited using the remote PEALD using DEZ precursor with oxygen plasma time of 4 s, RF power of 100 W, a pressure of 57.5 mTorr and an $O_2$ flow 60 *sccm* [2]. After deposition, the films were etched in anisotropic reactive ion $CHF_3$ etch to form thin-film at the sides of the $SiO_2$ as illustrated in Fig. 5.1(c). Aluminium source and drain contacts were evaporated and lifted off in NMP solution [2]. The contacts were annealed by a rapid thermal anneal (RTA) for 2 minute at 350 °C to improve the ohmic contact [2]. Al is used because the metal forms good ohmic contacts with ZnO because its work function of $\Phi_{AL} = 4.28$ eV which is close to the electron affinity of ZnO, $\chi$ of 4.29 eV. It was also found that Al has a better surface quality with ZnO than Ti which can reduce surface states. Optical microscope and SEM images were used to study the devices are shown in Fig. 5.2.

## 5.3 Electrical Characterisation of ZnO TFTs

Electrical characteristics of ZnO TFTs have been measured at PEPS laboratory Swansea University. Devices were connected by terminals needle probes connecting the gate followed by the source and the drain. The gate terminal is a metal plate below the substrate (back gate contact). All the set-up was carried out at room temperature [3].

### 5.3.1 Output Characteristics of ZnO TFTs

We have measured the drain current $I_D$ as a function of drain bias $V_D$ at gate biases, $V_G$, from 2-20 V. Fig. 5.3 (a, b, c, and d) shows output $I_D$-$V_D$ characteristics of ZnO thin-film FETs with different channel lengths ($L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m). These characteristics demonstrated an operation in $n$-type mode, normally-off device behaviour [4].

Devices (c) and (d) in Fig. 5.3 (c and d), with the channel lengths of 4 $\mu$m and 2 $\mu$m, clearly shown an ohmic behaviour compared to devices (a) and (b) in Fig. 5.3 (a and b) which are more saturated. When we increased the gate bias, we observed well the saturation region of ZnO FETs with channel lengths of 2 $\mu$m, and 4 $\mu$m. Moreover, the maximum attainable $I_D$ values increase proportionally with a decrease in the channel length ($L_{ch}$), as $L_{ch}$ decreases from 10 $\mu$m to 2 $\mu$m. The maximum $I_D$ is 57 nA, 92 nA, 192 nA, and 225 nA for 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m channel length transistors, respectively.

Output characteristics shown a well distinguished linear region at a low bias and saturation region at high bias. As the gate bias increases, the drain current increases with the increase of the drain voltage up to 5 V, When the transistor is turned on, by applying a gate bias, the channel is eventually created, which allows the current to flow between the drain and the source. The devices operate such as resistor, controlled by the gate voltage relative to both the source and drain voltages. In this region transistors behave an Ohmic behaviour [4]. In addition, when the gate bias increases up to 20 V, the devices shown a well-defined saturation behaviour as shown in Fig. 5.3 (a, b, c, and d). The electric field between the drain and the channel is very high and conduction continues [4]. The drain current is now weakly dependent upon a drain voltage and controlled primarily by the gate-source voltage.

### 5.3.2 Breakdown Voltages of ZnO TFTs

A breakdown voltage has been measured in carefully design experiments (associated with experiments in which the design introduces conditions that directly affect the variation, such as high voltage) to protect device functionality from unexpected burn out due to undue large applied bias [5]. Drain bias ($V_D$) has been increased slowly until the drain current promptly increased. The results from these investigations of a breakdown voltage for the TFTs are as shown in Fig. 5.4 (a, b, c, and d). Devices

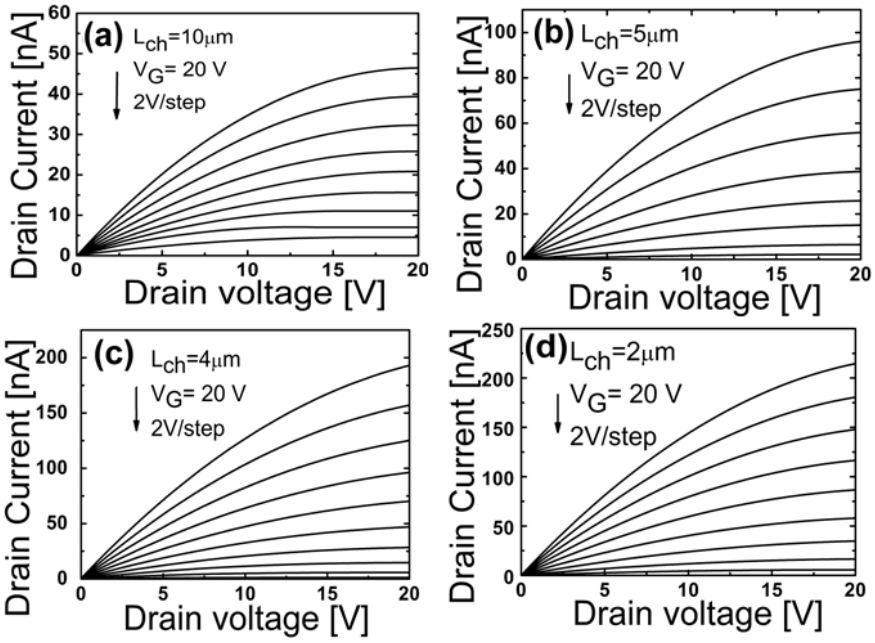


Figure 5.3: Output ($I_D$-$V_D$) characteristics from $V_G$ = 20 V to 2 V with a step of 2 V for ZnO TFTs with different channel lengths ($L_{ch}$) of (a) 10 $\mu$m, (b) 5 $\mu$m, (c) 4 $\mu$m, and (d) 2 $\mu$m, respectively.

with channel lengths of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m have exhibited breakdown voltages approximately 79.91 V, 70.07 V, 64.68 V, and 58.85 V for 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m channel lengths, respectively. These results are also collected in Table 5.1. This is relatively high breakdown voltages which are very promising for circuit applications with high drive voltage requirements such display panel and diode [5].

Table 5.1: Extracted breakdown voltage versus channel length for 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m.

| Channel length [$\mu$m] | Breakdown [V] |
|---|---|
| 10 | 79.91 |
| 5 | 70.07 |
| 4 | 64.68 |
| 2 | 58.86 |

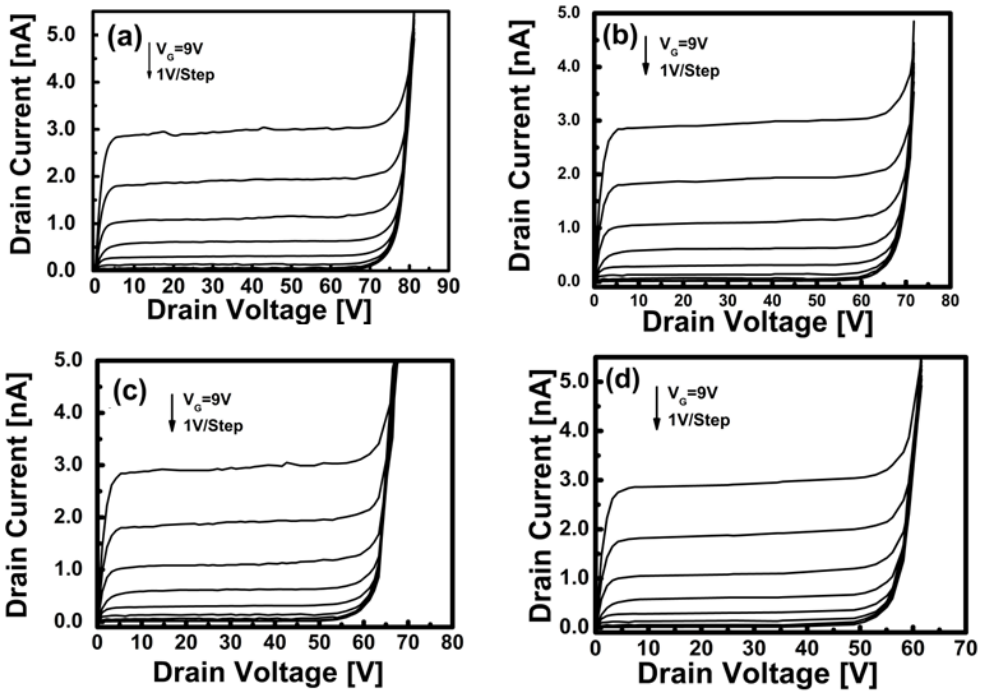


Figure 5.4: Output $I_D$-$V_D$ characteristic of a ZnO TFTs with a channel length $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m exhibiting a breakdown voltage 79.91 V, 70.07 V, 64.68 V, and 58.85 V, respectively.

### 5.3.3 The Effect of Channel Length Scaling on Current, Threshold and Sub-Threshold Regions of ZnO TFTs

To study the impact of channel length scaling on devices performance, Fig. 5.5 (a, b, c, and d) illustrates $I_D$ – $V_G$ characteristics for channel lengths of $L_{ch}$ =10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m at a drain bias $V_D$ = 5 V. The devices with the channel length $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m have demonstrated the values 3.6 $\mu$A, 27 $\mu$ A, 20 $\mu$ A and 17.2 $\mu$ A, respectively. It can be clearly seen that, the drain current increases by about 79.07 % when we decrease the channel length from 10 $\mu$m to 2 $\mu$m. Similar behaviour is seen when we scale down our channel length from 5 $\mu$m to 4 $\mu$m, the increase in the drain current is roughly about 25.93 %.

In the on-current region, a drain current ($I_D$) is dominated by a drift transport of carriers [6]. When the channel length of the ZnO TFTs is scaled down by decreasing the distance between the source and the drain, the electric field along the channel increases leading to increase in the acceleration of electrons by electric field in the channel. Consequently, injection of electrons from source into channel becomes also

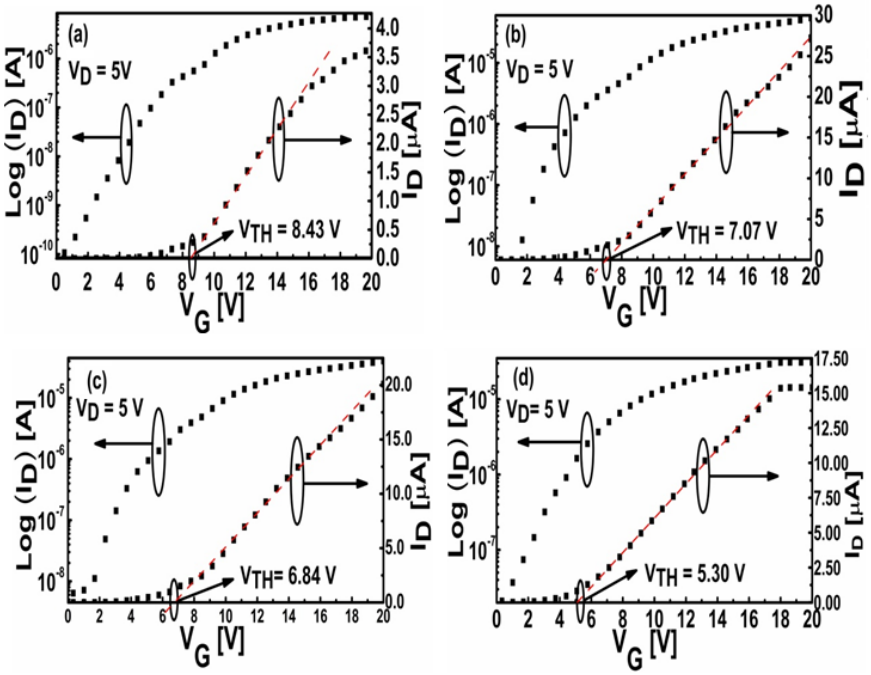


Figure 5.5: Transfer $I_D$-$V_G$ characteristics under a drain bias of $V_D = 5.0$ V for (a) 10 $\mu$m, (b) 5 $\mu$m, (c) 4 $\mu$m, and (d) 2 $\mu$m channel length ZnO TFTs, respectively.

more efficient since electrons gain larger kinetic energy to overcome potential barrier between the source and the drain by thermionic transport (electron tunnelling component is negligible due to the width of the potential barrier). This increase in the electron velocity accompanied by an increase in electron density is also the main reason for the increase in a maximum drain current when the channel of ZnO TFTs is scaled down from 10 $\mu$m to 5 $\mu$m, 4 $\mu$m and 2 $\mu$m.

We have investigated a threshold voltage when the source-to-drain distance defining the channel is scaled down [6]. Fig. 5.5 (a, b, c, and d) shows the channel length versus threshold voltage. The threshold voltage for the 10 $\mu$m and 5 $\mu$m channel length ZnO TFTs are 8.43 V, and 7.07 V, respectively at fixed $V_D = 5.0$ V. When the channel length further decreases to 4 $\mu$m and 2 $\mu$m, the threshold voltage decreases to 6.84 V and to 5.30 V, respectively, at the same $V_D = 5.0$ V. The sub-threshold region exhibits approximately a linear behaviour of current on logarithmic scale which indicates well behaved transistor with a small leakage current.

At $V_D = 5.0$ V, transistors with channel lengths of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m have sub-threshold slopes of 1.67 mV/dec, 0.75 mV/dec, 0.57 mV/dec, and 0.41 mV/dec, respectively. Therefore, the decrease in the sub-threshold slope of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m channel length TFTs is caused by decrease in channel length [6].

The sub-threshold characteristics are thus dependent on a channel length which agrees with the standard theory of Si MOSFETs [6]. In the sub-threshold region, drain current ($I_D$) is dominated by a diffusion transport of carriers and is inversely proportional to $L_{ch}$ [7]. The decrease in sub-threshold voltage with a decrease in channel length during the TFT scaling is caused by the increase in electron density in the channel [8]. This is because the ZnO TFT becomes a function in accumulation channel. Thus, because of the decrease in a channel length, it becomes easier to create an accumulation channel for a given gate bias that results a decrease in $V_{Th}$ as the channel length decreases [8].

### 5.3.4 Drain Induced Barrier Lowering of ZnO TFTs

The experimental results for drain induced barrier lowering (DIBL) versus gate voltage for physical channel length ($L_{ch}$) for 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m of ZnO TFTs are plotted in Fig. 5.6 (a, b, c, and d). The black spheres in Fig. 5.6 (a, b, c, and d) show the dependence between the drain current ($I_D$) and the gate voltage ($V_G$) when the drain voltage ($V_D$) is low (1.0 V), and the red spheres show the same dependence when the drain voltage is high (5.0 V). The DIBL is thus the difference in a threshold voltage when the drain voltage is increased from 1.0 V to 5.0 V.
Fig. 5.7 shows that, as the channel becomes shorter, the DIBL becomes more pronounced. If the channel length is decreased, the potential barrier in the channel increases as it can be seen in Fig. 5.7, which is showing the dependency between channel lengths and the DIBL. When the channel length is sufficiently large the source and drain junctions will be apart from each other such that they will not affect each other. By decreasing the channel length, the space charge at the drain will interact with that at the source which is leading to the potential barrier lowering at the source to the channel. As the channel becomes shorter this lowering becomes pronounced [9].

### 5.3.5 Total Resistance with Scaled Channel Length of ZnO TFTs

The total resistance $R_{Tot}$ has been extracted from the linear regime of $I_D$-$V_D$ characteristics for different channel lengths $L_{ch}$ 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m TFTs at two gate biases (10.0 V and 15.0 V step). Fig. 5.8 (a, b, c, and d) are shown the

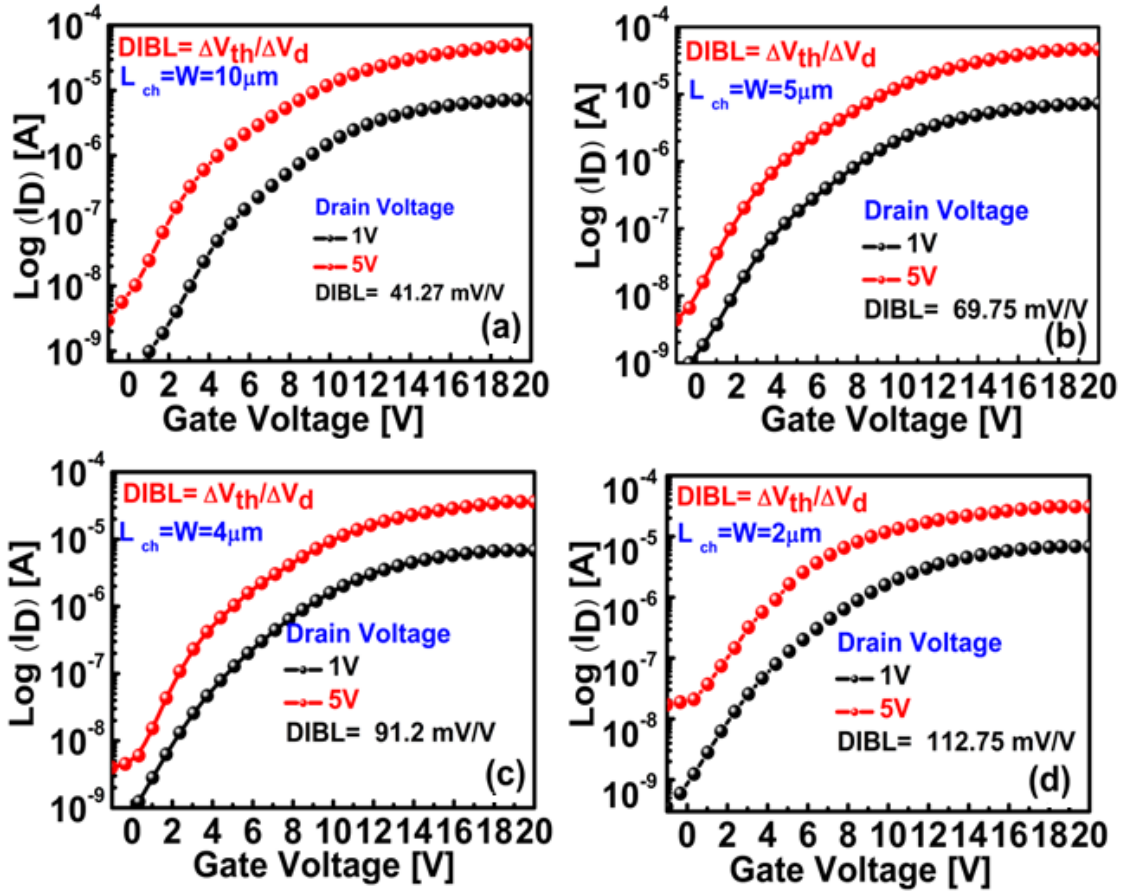


Figure 5.6: Extraction of DIBL from the drain current versus the gate voltage ($I_D$-$V_G$) characteristics of ZnO TFTs with different channel lengths of (a) $L_{ch}$ = 10 $\mu$m, (b) $L_{ch}$ = 5 $\mu$m, (c) $L_{ch}$ = 4 $\mu$m, and (d) $L_{ch}$ = 2 $\mu$m.

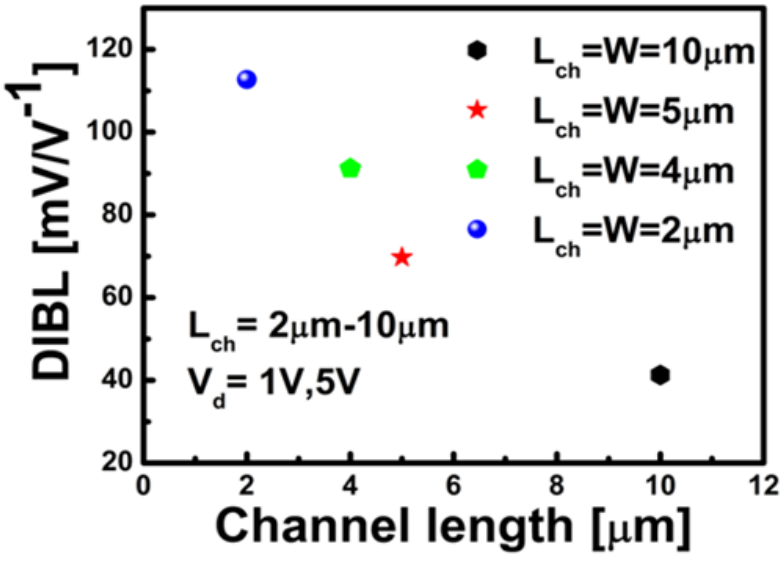


Figure 5.7: The DIBL of ZnO TFTs shows the increase with the decrease in channel lengths of $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m.

extracted total resistance at $V_G = 10$ ($V_G = 15$ V not included in the graph). We can clearly see that, in the linear operating regime, the resistance varies linearly with the channel length where the slope is proportional to the channel resistance as the channel length decrease from 10 $\mu$m to 2 $\mu$m the total resistance decreases this is due to the increase in surface scattering concentration which attribute to a large surface scattering which leads to more effective screening of impurity scattering. The carriers will also act as scattering centres that disrupt the flow of carriers in the channel and increase the total resistance due to remote Coulomb scattering. Since the resistance is proportional to the channel length, the increase in the channel length increases output resistance. Thus, $R_{\mathrm{Tot}}$ can be expressed linearly with dependence on the channel length $L_{\mathrm{ch}}$ [10]. The relation between total resistance and channel resistance can be expressed as:

$$R_{\mathrm{Tot}} = R_{\mathrm{C}} + R_{\mathrm{ch}} = R_C + \frac{L}{WC\ \mu_n V_D\ (V_G - V_{Th})} \tag{5.1}$$

Fig. 5.9 and Table 5.2 show the normalised total resistance for all transistors with different channel length $L_{\mathrm{ch}}$ for the 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m TFTs at two gate biases of 10.0 V and 15.0 V to be use in the transmission line method. The figure also shows the slope extraction for the normalised total resistance at two gate biases (10.0 V and 15.0 V). Fig. 5.9 shows also that the normalised total resistance for a 10 $\mu$m channel length ZnO TFT is three times larger as the total resistance resistance for the 2 $\mu$m channel length (the normalised total resistance becomes proportional to the channel length). This is because of more electrons contribute to the channel transport increasing an electron density in the channel region and near the contact allowing electrons with large kinetic energy to overcome Schottky barrier between metal and semiconductor efficiently thus lowering access resistance [11]. Therefore, the normalised total resistances is found to decreasing from 0.3659 $\Omega$ cm$^2$ measured at $V_G = 10.0$ V to almost 0.297 $\Omega$ cm$^2$ compared to measured at $V_G = 15.0$ V. The change of total resistance with gate potential my be due to source-drain contact overlap [12].

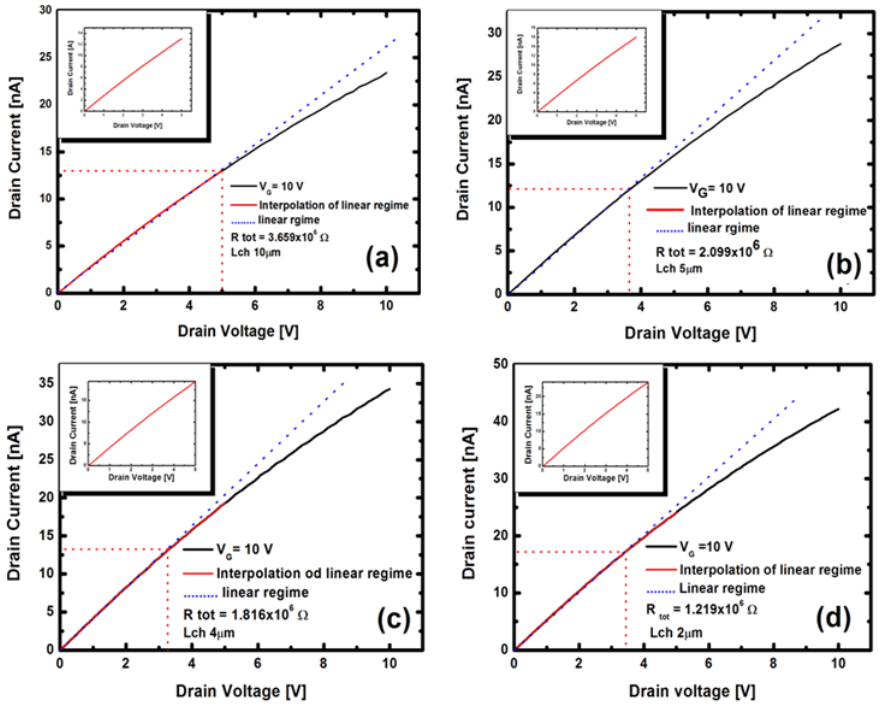


Figure 5.8: Total resistance for (a) the 10 $\mu$m ZnO TFT channel length, (b) the 5 $\mu$m ZnO TFT channel length, (c) the 4 $\mu$m ZnO TFT channel length, and (d) the 2 $\mu$m ZnO TFT channel length under a gate bias of $V_G$ = 10.0 V.

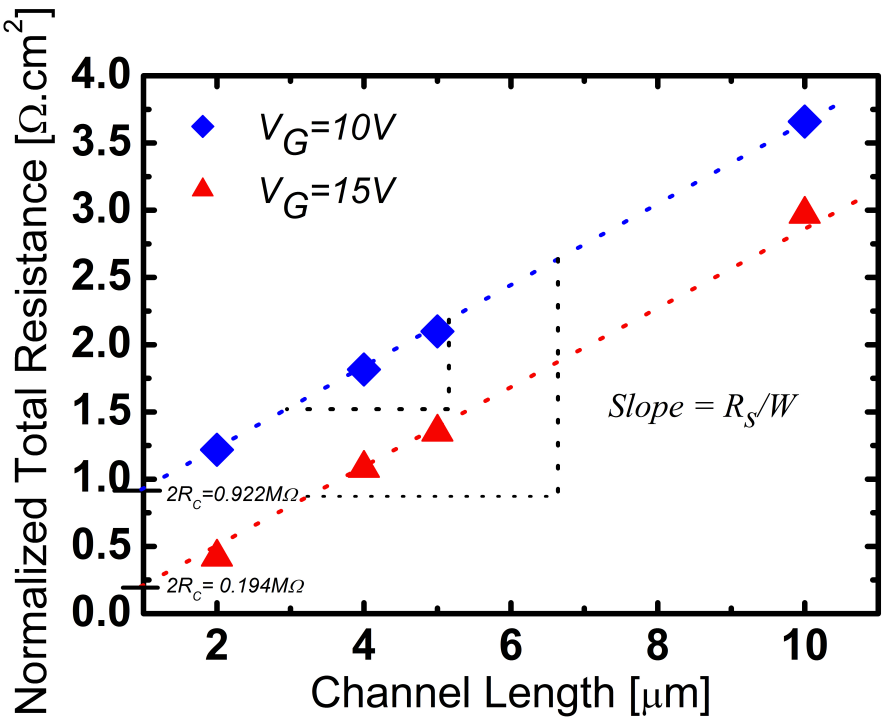


Figure 5.9: Normalised total resistance versus the channel length, $L_{ch}$ = 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m, at gate biases of $V_G$ = 10.0 V and 15.0 V. The dash lines are guide to the eyes.

### 5.3.6 Contact Resistance of ZnO TFTs

Electrons are flow from the source to the drain which are usually controlled by the applied gate voltage $V_G$. The applied gate voltage attracts the electrons to move at the interface region between the gate and the source-to-drain. These electrons form a conducting channel between the source and the drain, called the inversion layer [10]. Fig. 5.9 shows the normalised total resistance for different channel length ($L_{ch}$). To apply the TLM, a four point probes, where a constant current is supplied by three probes. The total resistance ($R_{\mathrm{Tot}}$) between two neighbouring contact pads and separated by a distance ($L$) is given by following equation:

$$R_{\mathrm{Tot}} = \frac{2R_s L_T}{W} + \frac{R_s L}{W} \tag{5.2}$$

where $R_s$ is the sheet resistance between the contact pads and under the contact pads, $L_T$ is the transfer length and refers to the distance across which most of the current transfers into the contact pads from the semiconductor and $W$ is the width of a device. Fig. 5.9 shows a plot of $R_{\mathrm{Tot}}$ as a function of $L$. $R_C$ is the contact resistance associated with a metal/semiconductor interface. $R_C$ can be obtained as a point at a plot of normalised total resistance versus ($R_{Tot}^{L=0}$) where we extrapolate the contact resistance at a channel length of zero ($L = 0$). Therefore, $R_C$ can be written as:

$$R_C = \frac{R_{Tot}^{L=0}}{2} \tag{5.3}$$

Note that the measured contact resistance $R_C$ can also be defined as:

$$R_{\mathrm{Tot}} = 2R_C + \frac{R_s L}{W} \tag{5.4}$$

The slope in Fig. 5.9 gives the value of $R_s/W$. The specific contact resistance $\rho_C$ from Eq. (5.4) becomes:

$$\rho_C = R_C\, W L_T \tag{5.5}$$

Since we calculated the specific contact resistance $\rho_C$ for ZnO TFTs with a different channel length. Now, we consider the contact resistance $R_C$, we re-arrange Eq. (5.5)

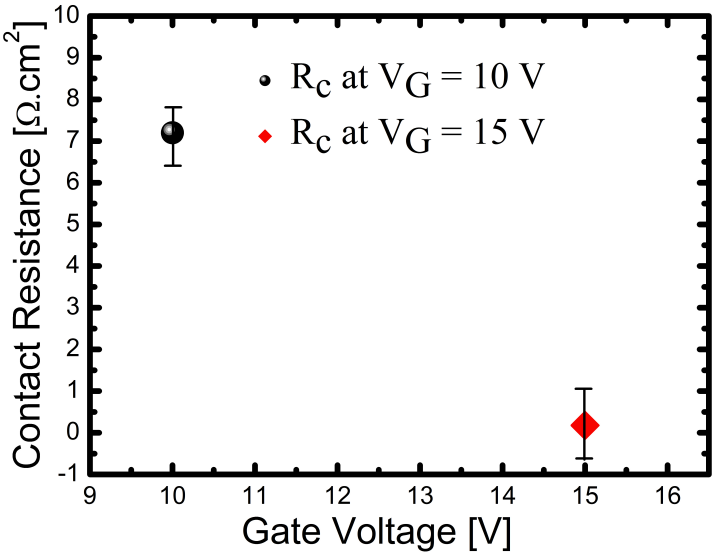


Figure 5.10: Contact resistance versus the gate voltage at different gate bias ($V_G$= 10.0 V and 15.0 V).

and use Eq. (5.2) for $L = 0.0$, then we obtain the following relation:

$$R_C = \frac{\rho_C}{W L_T} = \frac{R_s L_T}{W} \tag{5.6}$$

We calculated the contact resistance $R_C$ using Eq. (5.6). The contact resistance is about $7.2 \times 10^{-2}$ $\Omega$.cm$^2$, at gate voltage of 10.0 V. When the gate voltage is increased to 15.0 V, the contact resistance reduces to 0.177 $\times 10^{-2}$ $\Omega$.cm$^2$. This value is about 106.78 % smaller than the value obtained at 10.0 V gate voltage. This is because, when the gate voltage increases from 10.0 V to 15.0 V, the Schottky barrier height reduces at the source/drain resulting in more efficient accumulation of charges that contribute into carrier transport along the channel [7]. In order to normalise the contact resistance, the value of $R_C$ is multiplied by the width ($W$) to obtain a value in $\Omega$.cm$^2$.

### 5.3.7 Effective Mobility of ZnO TFTs

In order to calculate effective mobility, from the MOSFETs theory the general formula to calculate the mobility can be written as the following expression [13]:

$$I_D = \frac{W}{L} \mu_n C_{ox} V_D [V_G - V_{Th}] \tag{5.7}$$

We can use a linear approximation to calculate the electron effective mobility. By re-arranging Eq. (5.7), electron mobility $\mu_{\mathrm{n}}$ can be written as:

$$\begin{aligned} \mu_{\mathrm{eff}} &= \frac{I_D}{V_D}\frac{L}{WC_{ox}[V_G - V_{Th}]} \\ \mu_{\mathrm{eff}} &= \frac{1}{R_{Tot}}\frac{L}{WC_{ox}[V_G - V_{Th}]} \end{aligned} \tag{5.8}$$

where is $R_{Tot} = \dfrac{I_D}{V_D}$ is the slope, $W$ is the width of the device, $L$ is the length, $C_{ox}$ is the oxide capacitance and $\mu_{\mathrm{eff}}$ is the effective electron mobility. In the depletion region, the TFT capacitor consists of two capacitors in series, the oxide capacitor, $C_{ox}$, and the depletion layer capacitor, $C_{Si}$. Therefore, the total capacitance for the device can be described as:

$$\frac{1}{C_{Tot}} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}} \tag{5.9}$$

The capacitance of thin-film structure depends on the voltage (bias) on the gate. An applied positive gate voltage ($\mathrm{V_G}$) larger than the flat band voltage ($\mathrm{V_{FB}}$) ($\mathrm{V_G} > \mathrm{V_{FB}}$) induces a positive charge on the metal gate and a negative charge in the semiconductor [14]. Total gate capacitance $\mathrm{C_G}$) is the oxide capacitance per unit area $\mathrm{C}_{ox}$ [15], which is given by:

$$\begin{aligned} C_{\mathrm{G}} &= C_{ox}A \\ &\text{or} \\ C_{Si} &= \frac{\varepsilon_{Si}\epsilon_0}{t_{Si}} \\ &\text{and} \\ C_{ox} &= \frac{\varepsilon_{Si}\epsilon_0}{t_{Si}} \end{aligned} \tag{5.10}$$

where $A$ is the area of the bottom gate, $\varepsilon_r$ is the relative static permittivity (also called the dielectric constant) of the material (for a vacuum, $\varepsilon_r = 1$), $\varepsilon_0$ is the permittivity of vacuum ($\varepsilon_0 \approx 8.854 \times 10^{-12}$ $\mathrm{F.m^{-1}}$), and $\mathrm{t}_{ox}$ is the oxide thickness. For the ZnO TFTs, $\mathrm{t}_{Si}$ = 5.5 nm [2], $\mathrm{t}_{SiO_2}$= 100 nm, $\varepsilon_r$ for $SiO_2$= 3.9 and $\varepsilon_r$ for Si= 11.68 [2]; $\mathrm{C_{Tot}}$= $0.339{\times}10^{-6}$ $\mathrm{Fcm^{-2}}$. By substituting into Eq. (5.9), we can determine a total capacitance for the TFT as $\mathrm{C_{Tot}}$= $0.339{\times}10^{-6}$ $\mathrm{Fcm^{-2}}$. We can

calculate effective mobility of the 10 $\mu$m TFT FET at $V_{\mathrm{D}} = 5.0$ V as:

$$\begin{aligned} \mu_{\mathrm{eff}} &= \frac{I_D}{V_D}\frac{L}{WC_{ox}[V_G - V_{Th}]} \\ &= 3.65 \times 10^{-6}\frac{10 \times 10^{-4}cm}{0.339 \times 10^{-6}Fcm^{-2}.35 \times 10^{-4}cm.5V} \\ &= 0.11\ cm^2V^{-1}S^{-1} \end{aligned} \tag{5.11}$$

The electron effective mobility extracted for 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m channel length TFTs at two different biases (10.0 V, 15.0 V) is plotted in Fig. 5.11. The mobility increases with a decrease in the channel length at $V_{\mathrm{G}}$=10.0 V and 15.0 V. The electron mobility increases with the gate voltage increase due to the increase in kinetic energy of electrons which allows them to be de-trapped more efficiently from expected surface traps [16, 7]. In other words, when the gate voltage increases from 10.0 V to 15.0 V, the electric field along the channel increases leading to increase in the acceleration of electrons by electric field. Therefore, mobility increases. The carriers trapped at surface will act as scattering centres that interact with the flow of mobile carriers in the channel due to remote Coulomb scattering. We can also notice that the electric field in the channel is reversely proportional to the channel length, leading to higher carrier velocities at reduced channel length, as defined by ($v = \mu E$). The values are collected in Table 5.3.

Table 5.2: Effective electron mobility extracted using Eq. (5.8), mobilities are decrease with channel lengths ($L_{\mathrm{ch}}$) of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m increased at two different gate biases of $V_{\mathrm{G}}$ = 10 V and 15 V.

| Channel length | 10 $\mu$m | 5$\mu$m | 4 $\mu$m | 2 $\mu$m |
|---|---|---|---|---|
| Effective electron mobility at $V_{\mathrm{G}}$ =10.0 V (cm$^2$/Vs) | 0.11 | 1.28 | 1.77 | 2.9 |
| Effective electron mobility at $V_{\mathrm{G}}$ =15.0 V (cm$^2$/Vs) | 0.38 | 2.86 | 3.25 | 4.04 |

### 5.3.8 Channel Mobility of ZnO TFTs

Channel electron mobility $\mu_{ch}$ is an essential parameter for field effect transistors [11] as it quantifies the semiconductor channel length performance with respect to the current drive capability [11]. The $\mu_{ch}$ influences the MOSFETs performance through the carrier velocity and the driving current. It is widely used for benchmarking different processes in technology development [11]. When the channel charge is fairly

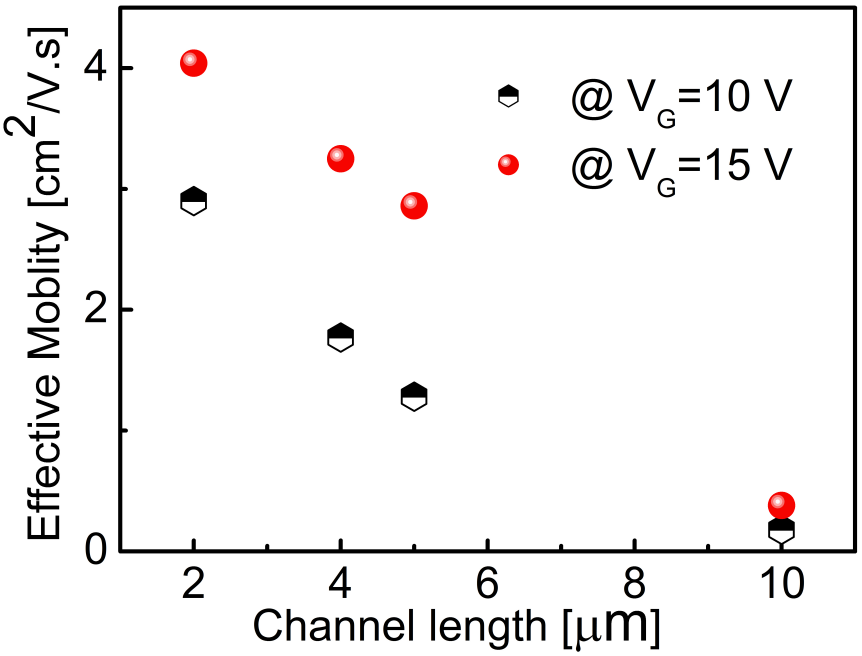


Figure 5.11: Effective electron mobility extracted using. The electron mobility decreases with increasing of the channel length at $V_G$=10.0 V and 15.0 V.

uniform from source to drain in the linear region, the channel effective mobility ($\mu_{ch}$) can be written as:

$$\mu_{ch} = \frac{I_{\mathrm{D}}}{V_{\mathrm{D}}} \frac{L}{W.Q} \tag{5.12}$$

where $Q$ is the charge in the channel. By considering the channel resistance, we can re-arrange Eq. (5.13) using MOSFET theory to be written as:

$$\mu_{ch} = \frac{L}{W} \frac{1}{Q_{\mathrm{inv}} R_{\mathrm{ch}}} \tag{5.13}$$

where $R_{\mathrm{ch}} = \mathrm{V_D/I_D}$ is the channel resistance. The inversion charge density per unit area $\mathrm{Q_{inv}}$ can be determine from the basic transistor equation:

$$Q_{inv} = C_{ox}[V_G - V_{Th}] \tag{5.14}$$

where is $\mathrm{V}_G \gg \mathrm{V}_{Th}$. Since $\mathrm{Q_{inv}} = 4.322{\times}10^{-6}\mathrm{C/cm^2}$ for the 10 $\mu$m device channel length, channel mobility can be calculated for each channel length.

We calculated the channel resistance ($R_{ch}$) for each channel length ($L_{\mathrm{ch}}$) by using

Table 5.3: Channel resistance extracted using Eq. (5.1), channel resistances are increasing with channel lengths ($L_{\mathrm{ch}}$) of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m increased at two different gate biases of $\mathrm{V_G}$ = 10.0 V and 15.0 V.

| Resistance | 10 $\mu$m | 5 $\mu$m | 4 $\mu$m | 2 $\mu$m |
|---|---|---|---|---|
| Channel Resistance at $\mathrm{V_G}$ =10.0 V ($\Omega$) | 0.296 | 0.1398 | 0.112 | 0.0518 |
| Channel Resistance at $\mathrm{V_G}$ =15.0 V ($\Omega$) | 0.279 | 0.1173 | 0.090 | 0.0243 |

Eq. (5.1) at a different gate bias ($\mathrm{V}_G$= 10.0 V and 15.0 V) as we summarised these values in Table 5.3. Since we extracted the channel resistance ($R_{ch}$), we can calculate the channel mobility for each device as we will discuss later on in this chapter. The channel mobility can be obtained from Eq. (5.13). For channel length 10 $\mu$m $\mu_{ch}$:

$$= \frac{10 \times 10^{-4} cm}{4.322 \times 10^{-6} C/cm^2 \times 10 \times 10^{-4} cm \times 0.296 \times 10^6} = 0.782\ cm^2 V^{-1} S^{-1} \quad (5.16)$$

Table 5.4: Channel electron mobility extracted using Eq. (5.14), mobilities are increasing rapidly with channel lengths ($L_{\mathrm{ch}}$) of 10 $\mu$m, 5 $\mu$m, 4 $\mu$m and 2 $\mu$m increased at two different gate biases of $\mathrm{V_G}$ = 10.0 V and 15.0 V.

| Channel length | 10 $\mu$m | 5$\mu$m | 4 $\mu$m | 2 $\mu$m |
|---|---|---|---|---|
| Channel Electron Mobility at $\mathrm{V_G}$ =10.0 V ($\mathrm{cm^2/Vs}$) | 0.782 | 8.28 | 8.30 | 8.9 |
| Channel Electron Mobility at $\mathrm{V_G}$ =15.0 V ($\mathrm{cm^2/Vs}$) | 0.83 | 9.86 | 10.25 | 19.04 |

Similarly, channel mobility at gate bias 15.0 V has been calculated and plotted in Fig. 5.12. The gate voltage increase from 10.0 V to 15.0 V makes the electric field along the channel larger increasing acceleration of electrons by electric field which increases the electron mobility. The mobility also increases with a decrease in the channel length at $\mathrm{V_G}$=10.0 V and 15.0 V. The values are collected in Table 5.4. Fig. 5.12 shows that the extracted channel electron mobility of ZnO TFTs increases with the decreasing of the channel length. The channel mobility however increases when comparing values at gate biases of 10.0 V and 15.0 V. The channel mobility

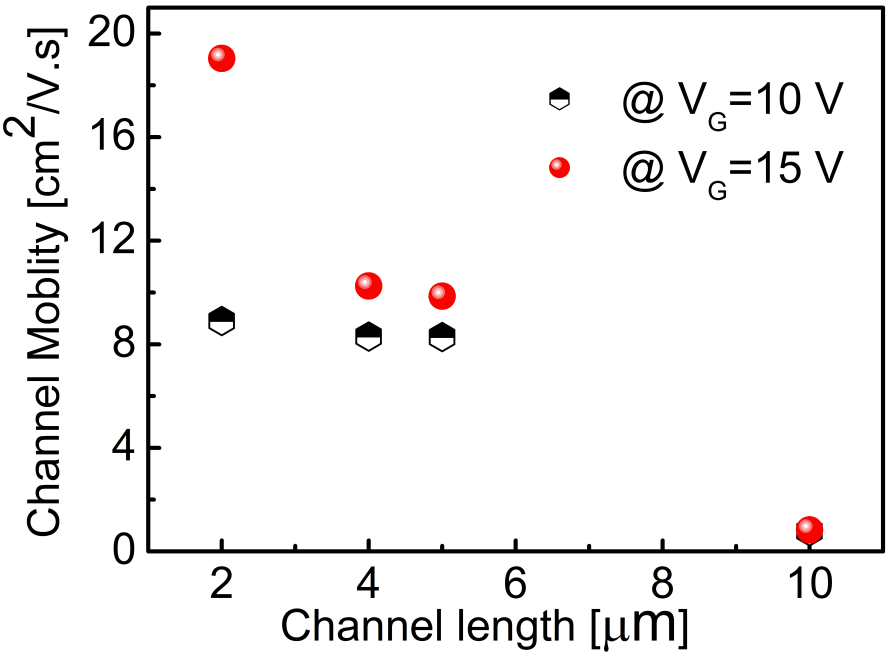


Figure 5.12: Channel electron mobility extracted using Eq. (5.14), channel mobility shows that increasing rapidly with increased channels length at gate biases of $V_G$ = 10.0 V and 15.0 V.

will increase from 0.782 to 0.83 $cm^2$/Vs by about 6 % for the 10 $\mu$m channel length TFTs, from 8.28 $cm^2$/Vs to 9.86 $cm^2$/Vs for 5 $\mu$m channel length by about 16 % from 8.30 to 10.25 $cm^2$/Vs (about 13 %) for the 4 $\mu$m channel length, and from 8.9 $cm^2$/Vs to 19.04 $cm^2$/Vs (around 53 %) for the 2 $\mu$m channel length. The increase of the electron channel mobility during the channel scaling is indicative of a reduced electron scattering due to the increase in electric field along the channel. This reduction in the carrier scattering increases electron velocity because electrons will have a longer mean-free path in the scaled thin-film channels.

## 5.4 ZnO NW-FETs Fabrication

### 5.4.1 Remote Plasma Enhancement Atomic Layer Deposition

The technique is cyclic, based on two self-limiting reactions, metallization and oxidation. These reactions are separately executed on the surface substrate. In addition, the diethyl zinc (DEZ) was used as the zinc metal precursor during the metalliza-

tion. When the DEZ adsorbs the surface substrate, the absorbed DEZ reacts with the oxidant in the oxidation steps [2]. Usually, the oxidant is a water which is widely known as a thermal ALD [17]. To execute the reactions separately, pump and purge steps are implemented between the metallization and oxidation steps. In each ALD cycle (steps), the surface was ideally left with one mono-layer of ZnO [2]. The ZnO film is thermally grown on a 100 nm $SiO_2$/*p*-Si substrate to a thickness of about 100 nm. The grown Si and $SiO_2$ are cleaned in acetone and iso-propyl alcohol (IPA) ultrasonically for 1 min, respectively, in order to avoid solution residues on cleaned components. Finally, the samples are immediately loaded into the reactor to cool until they reached room temperature for the RIE process [17].

### 5.4.2 Top-Down Fabrication of ZnO NW-FETs

The top-down fabrication method starts with a thin film deposition by Remote Plasma Enhanced ALD (PEALD). The PEALD is followed by aniso-tropically reactive ion etch (RIE) to produce ZnO NWs with different channel lengths (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m). Optical and electrical characterisations is then carried out to study a scaling of channel length ($L_{ch}$) in the transistors. The fabrication process starts with a *p*-type silicon wafer, which is used as a substrate and back-gate as it is shown in Fig. 5.14(a). The wafer is cleaned in a fuming nitric acid for 15 minutes and dipped in a hydrofluoric acid. A 100 nm $SiO_2$ layer is grown by a dry thermal oxidation as a gate insulator as seen in Fig. 5.14(a). An 80 nm (measured by ellipsomerry) layer of ZnO was then deposited at 190 °C using remote plasma ALD in Oxford Instrument plasma technology (OIPT) Flex-Al system with diethyl zinc as the precursor, and RF power of 100 W, a pressure of 80 mTorr, and an $O_2$ flow of 60 sccm, as shown in Fig. 5.14(b) [2]. The ZnO NWs top-down fabrication described here uses a mature >1 $\mu$m photo-lithography and anisotropic reactive ion etching (RIE). This process is carried out by different steps [2]. Fig. 5.15 illustrates a schematic structure of this top-down fabrication. The top inset shows SEM of the selected area of two NWs horizontally aligned on the Al Pad.

The advantage of using the remote plasma ZnO ALD compared to water-based oxidation is the reduction of OH impurities, which can increase the film resistivity. The ZnO NWs was defined by photo-lithography and anisotropic inductively coupled plasma (ICP) etching based on $CHF_3$ gas chemistry. Finally, a 500 nm thick Al metal

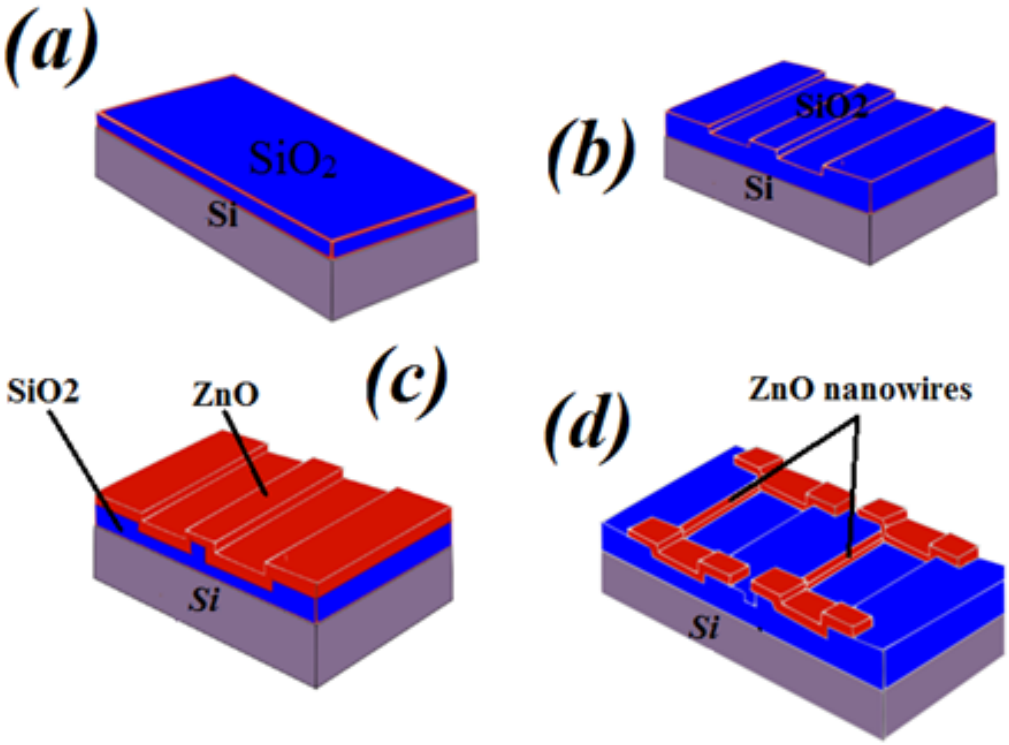


Figure 5.13: Top-down fabrication process of ZnO NW-FETs, (a) a *p*-type silicon wafer as a substrate and a dry thermal oxidation grow of 100 nm $SiO_2$ layer, (b) photo-lithography and anisotropic RIE to form a 100 nm trench, (c) ZnO thin film deposited by a remote plasma and dry etched to form the NWs, and (d) final fabricated ZnO NW-FETs.

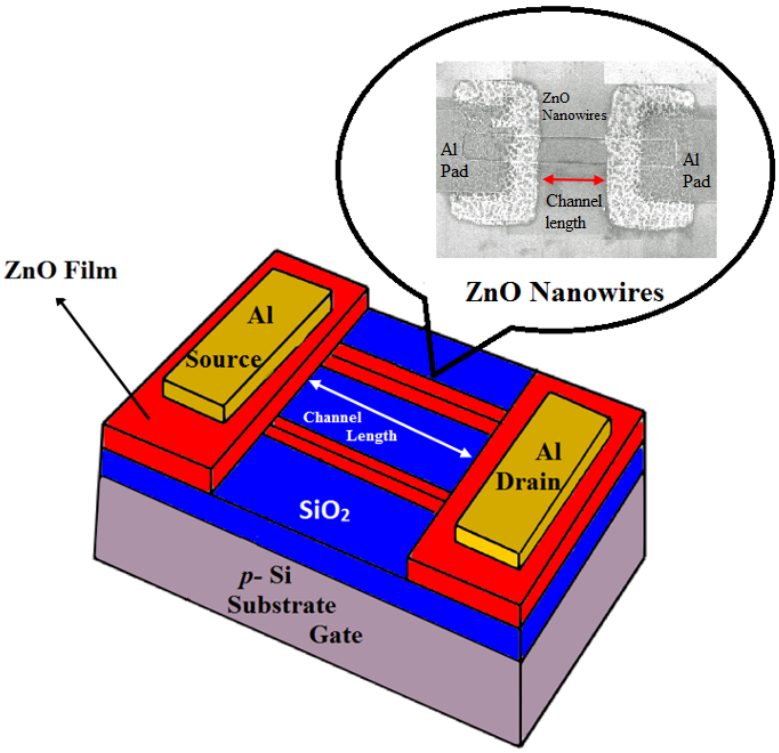


Figure 5.14: Schematic illustration of the top-down fabrication process of ZnO NW-FETs. The inset shows the SEM of the two identical NWs across the Al pad.

electrode was deposited by an electron beam evaporation and lift-off as source and drain contacts. The Al contacts were then annealed at 350 °C for 2 minutes to improve the ohmic contact. Al has a work function, $\Phi_{Al} = 4.28$ eV which is close to the electron affinity of ZnO (4.29 eV). It was also found that Al has a better surface quality with ZnO than titanium (Ti) which can reduce surface states [2].

In addition, the NWs with various lengths can be fabricated in a well-defined locations on the substrate. Although bottom-up process provides a good morphology, a large aspect ratio, and a high crystallinity, this technique sometimes generate a random alignment for NWs on a substrate [18].

The main advantage of top-down fabrication is to resolve a large number of bottom-up technique problems. This is can be control the size and the location of NWs. The process also can provide a large aspect ratio, a good morphology, and a high crystallinity for the NWs. However, the technique has shown a significant variation of electrical characteristics, such as a variation in a field effect mobility and in an output drain current when obtained from ZnO nanowire field effect transistors

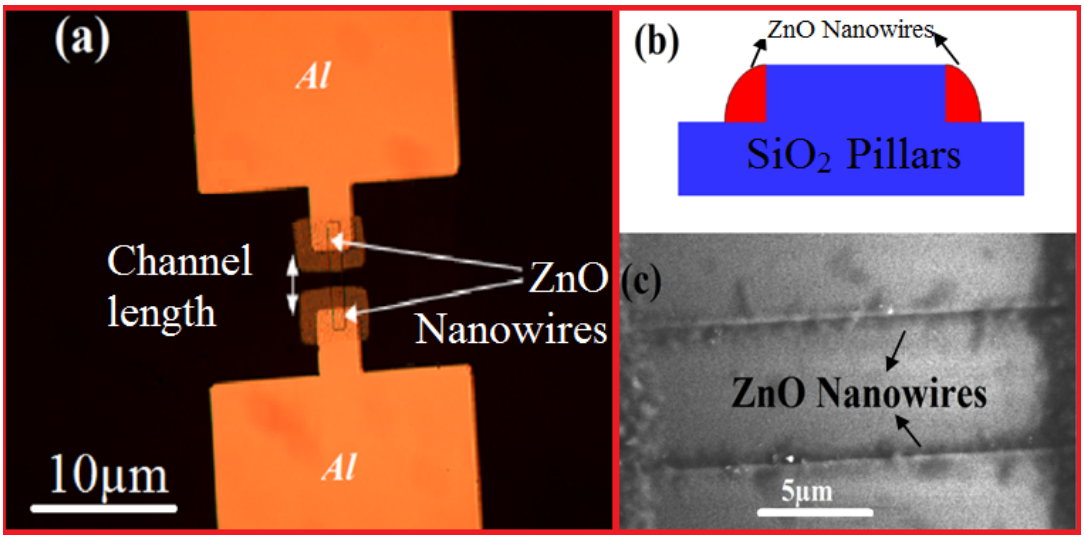


Figure 5.15: (a) Optical microscope views a pair of ZnO NWs in contact with Al pad. (b) Optical image of two NWs with an approximative height of 80 nm. This value was determined by the height of the $SiO_2$ pillar and the amount of over-etch of the ZnO layer. (c) A pair of NWs from SEM after the RIE etch.

(NW-FETs) as we shown in chapter 2.

## 5.5 Electrical and Optical Characterisation of ZnO NW-FETs

### 5.5.1 Optical Properties of ZnO NW-FETs

To study the optical characteristic of nano-films [19]. Fig. 5.16(a) shows the two fabricated NWs with a channel length of 2 $\mu$m. The width and height of the ZnO NWs are 40 nm and 80 nm, respectively, These dimensions can be controlled by adjusting the thickness of the ZnO layer and the height of the $SiO_2$ trench because of the ZnO NWs are formed at the side of $SiO_2$ pillars. Fig. 5.16(a) illustrates a successful formation of a spacer at oxide side [2]. Each NW height is approximately 80 nm, the value was determined by the height of the $SiO_2$ pillar and the amount of over-etch of the ZnO layer (by 20 % in this case) as it shown in Fig. 5.16 (b). Furthermore, Fig. 5.16 (c) shows a pair of NWs using the SEM after the RIE etch. The width of the NW is approximately 40 nm. This value is about 14 % thicker than the 35 nm deposited ZnO thin film transistors we have discussed earlier in the previous section.

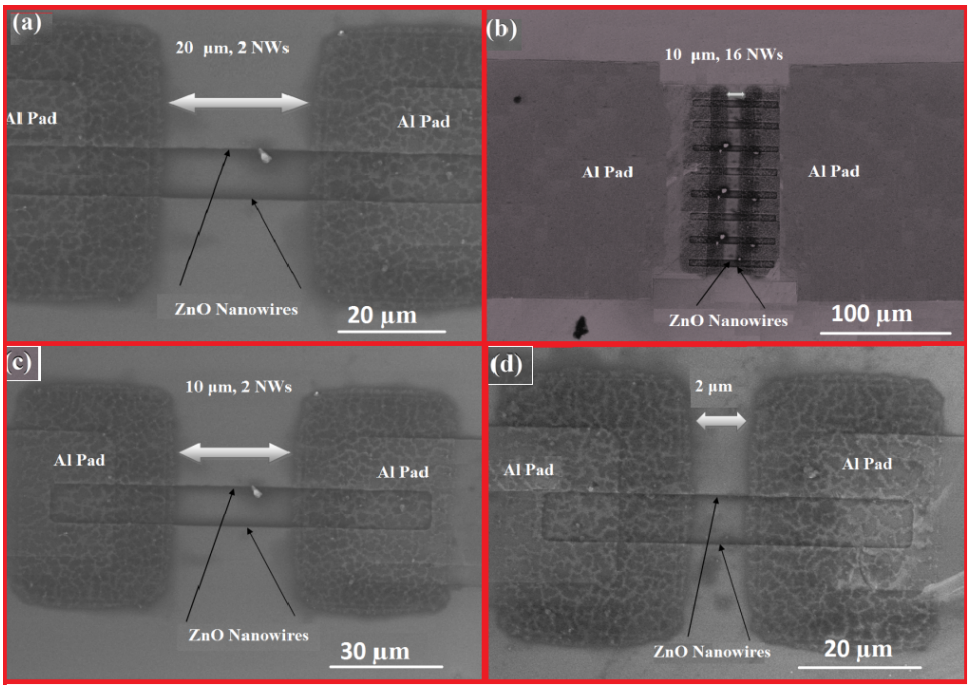


Figure 5.16: SEM cross-sectional view of ZnO NWs fabricated on a $SiO_2$/Si substrate with (a) a channel length of 20 $\mu$m with 2 NWs, (b) a channel length of 10 $\mu$m with 16 NWs, and (c) a channel length of 10 $\mu$m with 2 NWs, and (d) a channel length of 2 $\mu$m with 2 NWs.

#### Scan Electronic Microscope of ZnO NW-FETs

Fig. 5.17 (a, b, c, and d) shows cross-sections of the prepared ZnO NWs arrays of 20 $\mu$m (2 NWs), 10 $\mu$m (16 NWs), 10 $\mu$m (2 NWs), and 2 $\mu$m, respectively. The scan electronic measurement (SEM) shows that the NWs are closely packed and horizontally aligned onto Al pad and the Si substrate. Furthermore, Fig. 5.17(b) shows a schematic of NWs height determined by the height of the $SiO_2$ pillars and the amount of over-etch. This leads to the assumption that the $SiO_2$ surface left after the RIE etch due to the prolonged ion bombardment [2].

### 5.5.2 Output Characteristics of ZnO NW-FETs

Output $I_D$ – $V_D$ characteristics are measured at gate biases $V_G$ = (0.0 – 20.0 V). Fig. 5.18 (a, b, c, and d) shows output characteristics of ZnO NW-FETs with different channel lengths ($L_{ch}$) = 20 $\mu$m (2 NWS), 10 $\mu$m (16 NWs), 10 $\mu$m (2 NWs), and 2 $\mu$m (2 NWs). The $I_D$-$V_D$ characteristics exhibited a typical transistor behaviour of $n$-type enhancement mode. The output characteristic also shows a well distinguished linear region at low bias and a saturation region at a high bias. Furthermore, the maximum attainable $I_D$ increases proportionally with the decrease in

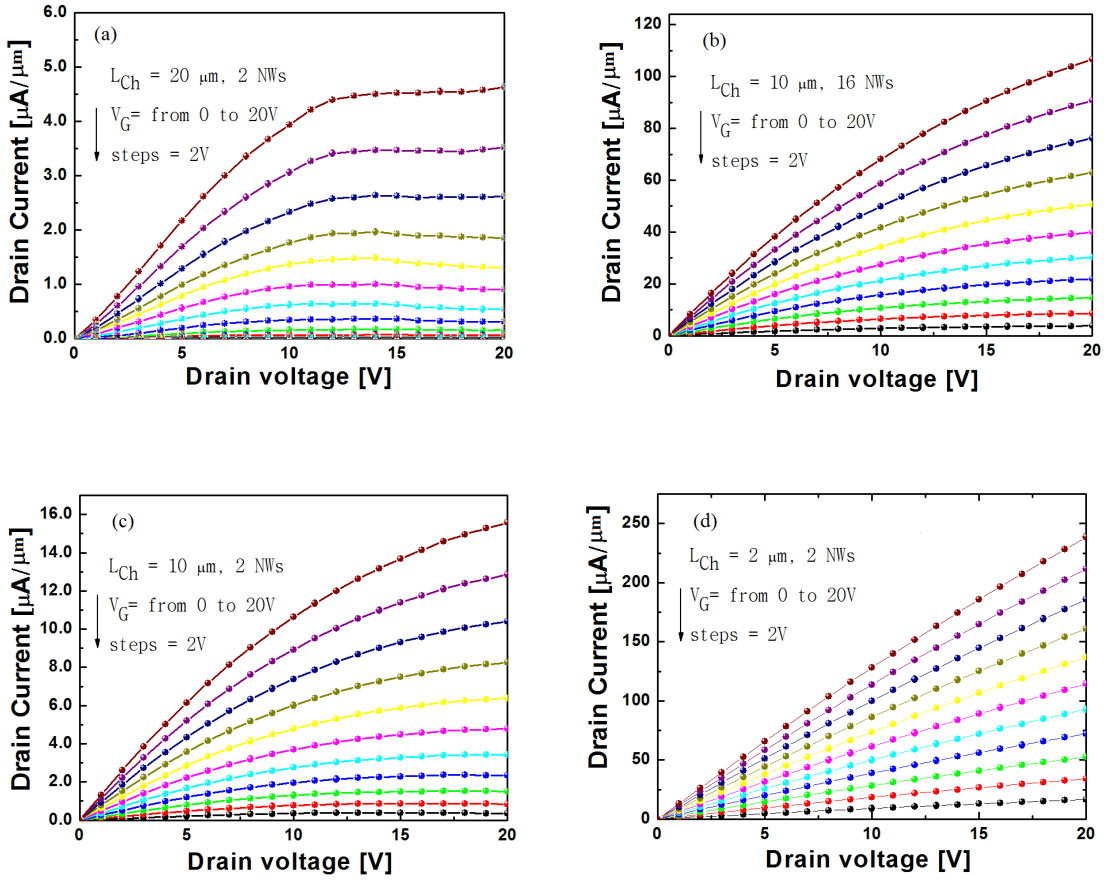


Figure 5.17: Transfer $I_D$-$V_G$ characteristics under a drain bias of $V_D$ = 5 V for ZnO NWs with different channel lengths $L_{ch}$ of (a) 20 $\mu$m (2 NWs), (b) 10 $\mu$m (16 NWs), (c) 10 $\mu$m (2 NWs), and (d) 2 $\mu$m (2 NWs), respectively.

the channel lengths ($L_{ch}$). As $L_{ch}$ decreases from 20 $\mu$m to 2 $\mu$m, the maximum $I_D$ increases as 5.8 nA, 15.85 nA, 192 nA, and 225 nA for 20 $\mu$m, 10 $\mu$m (2 NWs), 10 $\mu$m (16 NWs) and 2 $\mu$m, respectively. Notably that the current is normalized by the total perimeter of the NWs. The poor saturation of the drain current and $I_D$-$V_D$ characteristics dominated by an ohmic behaviour as seen in Fig. 5.18 (a) for 2 $\mu$m channel length transistor suggests the presence of short-channel effects. Similar behaviour has been observed earlier for 2 $\mu$m channel length ZnO thin-film transistors. Moreover, in order to observe a more saturation, we have increased the gate bias from 20.0 V to 40.0 V for 2 $\mu$m channel length device. The device has exhibited a good saturation of the drain current after the gate bias increased up to 40 V [20] as it shows in Fig. 5.19. This indicates to an excellent process compatibility with conventional FETs.

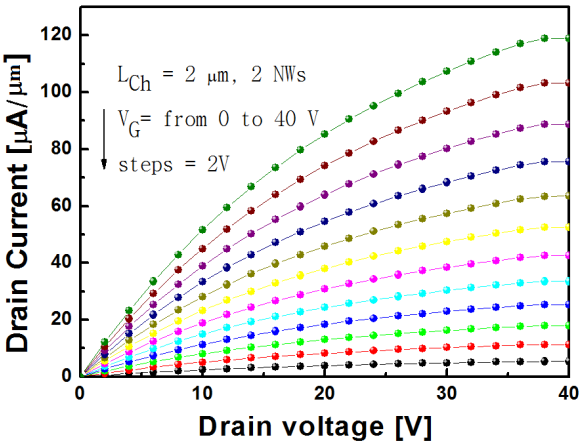


Figure 5.18: Output $I_D$-$V_D$ characteristics from $V_G$ = 40.0 V to 2.0 V with a step of 2.0 V for the ZnO NWs with a channel length $L_{ch}$ of 2 $\mu$m (2 NWs).

## 5.6 Transfer Characteristics of ZnO NW-FETs

Fig. 5.20 (a, b, c, and d) shows the transfer characteristics of devices with the channel length of $L_{ch}$ = 20 $\mu$m (2 NWs), 10 $\mu$m (2 NWs), 2 $\mu$m (2 NWs) and 10 $\mu$m (16 NWs) at $V_D$ = 1 V and 5.0 V. The measured current divided by the number of NWs, and the current per NW was normalized. We have shown the impact on the drain current of scaling down of a channel length by plotting $I_D$-$V_D$ characteristics at low and high drain bias (1.0 V and 5.0 V) for channel lengths of $L_{ch}$ = 20 $\mu$m (2 NWs), 10 $\mu$m (2 NWs) and 2 $\mu$m (2 NWs). At a low drain bias ($V_D$= 1.0 V), the drain current is 0.85 $\mu$A, 2.8 $\mu$A, and 4.2 $\mu$A for channel lengths of $L_{ch}$ = 20 $\mu$m (2 NWs), 10 $\mu$m (2 NWs), and 2 $\mu$m (2 NWs), respectively.

Similarly, when we increase the drain voltage up to 5.0 V, the devices have the drain current of 1.15 $\mu$A, 3.7 $\mu$A and 4.8 $\mu$A for the channel lengths of $L_{ch}$ = 20.0 $\mu$m (2 NWs), 10 $\mu$m (2 NWs), and 2 $\mu$m (2 NWs), respectively. Fig. 5.20 (a, b and c) shows that the drain current increases when the gate bias increases from 1.0 V to 5.0 V. At a low bias (1 V), the drain current increases from 0.85 $\mu$A to 2.8 $\mu$A by about 106 % when the channel length decreases from 20 $\mu$m (2 NWs) to 10 $\mu$m. Its also increases from 2.8 $\mu$A to 4.2 $\mu$A by about about 40 % when the channel length is reduced from 20 $\mu$m (2 NWs) to 10 $\mu$m (2 NWs). We have also compared the 20 $\mu$m (2 NWs) channel length and the 2 $\mu$m (2 NWs) (a short channel length and a long channel length) transistors. The drain current increases from 0.85 $\mu$A to 4.2 $\mu$A (about 133 %) when we scale the devices from 20 $\mu$m (2 NWs) to 2 $\mu$m (2 NWs). A similar behaviour is observed when we increase the drain bias to 5 V.

The drain current increases about 105 % and 26 % when the channel length decrease from 10 $\mu$m (2 NWs) to 2 $\mu$m (2 NWs), and, finally, the increase in the drain current is by about 123 % when we scale the device channel from 20 $\mu$m (2 NWs) to 2 $\mu$m (2 NWs).

Furthermore, the device with a same channel length (10 $\mu$m) and different NWs (2 NWs and 16 NWs), observed a drain current of 2.8 $\mu$A for 2 NWs and 20.1 $\mu$A for (16 NWs) at 1.0 V, when the drain voltage increases up to 5.0 V the device demonstrated the values of 3.7 $\mu$A 2 NWs and 32.6 $\mu$A for 16 parallel NWs, we can clearly see that, the $\times$ 8 difference in current demonstrates the fact of drain current scales down due to the effect of the NWs [2].

When the channel length of the ZnO TFTs is scaled down by decreasing the distance between the source and the drain, the electric field along the channel increases leading to increase in the acceleration of electrons by electric field in the channel [21]. Consequently, the injection of electrons from source into the channel becomes also more efficient since the electrons gain larger kinetic energy to overcome the potential barrier between the source and the drain by thermionic transport (electron tunnelling component is negligible due to the width of the potential barrier [22]. This increase in the electron velocity accompanied by an increase in electron density is also the main reason for the increase in a maximum drain current.

### 5.6.1 Impact of Channel Length on Threshold Voltage of ZnO NW-FETs

We have studied the impact of scaling down the channel lengths on threshold voltage at low and high drain bias (1.0 V and 5.0 V) for channel length of $L_{\text{ch}}$ = 20 $\mu$m (2 NWs), 10 $\mu$m (2 NWs), 10 $\mu$m (16 NWs) and 2 $\mu$m (2 NWs). At a low drain bias ($V_D$= 1.0 V), the threshold voltage demonstrated the values of 6.7 V, 5.9 V, 5.3 V and 4.7 V for channel lengths of $L_{\text{ch}}$ = 20 $\mu$m (2NWs), 10 $\mu$m (16 NWs), 10 $\mu$m (2 NWs) and 2 $\mu$m (2 NWs) respectively. When the drain bias increases up to 5.0 V, the threshold voltage exhibit values of 8.3 V, 7.6 V, 5.65 V, and 5.03 V for channel lengths of $L_{\text{ch}}$ = 20 $\mu$m (2 NWs), 10 $\mu$m (16 NWs), 10 $\mu$m (2 NWs) and 2 $\mu$m (2 NWs), respectively.

When the long channel length (10 $\mu$m) is compared to the short channel length (2 $\mu$m) transistors, the threshold voltage increases by 12 % When the drain bias

increases up to 5 V, the threshold voltage increases by about 11 % for a channel length of 2 $\mu$m (2 NWs). Table 5.5 shows that the threshold voltage decreases by 29.58 % when a long channel length (20 $\mu$m) transistor is reduced to a short channel length (2 $\mu$m) transistor. When the bias increases to 5.0 V, a threshold voltage decreases by 36.14 % from the value in the transistor with a channel length of 20 $\mu$m (2 NWs) to the one with a channel length of 2 $\mu$m (2 NWs).

The impact of scaling down the channel length on transfer characteristics is illustrated in Fig. 5.20 (a, b, c, and d). The charge distribution in the channel is strongly influenced by the field originating from the source/drain and the depletion region around the source and the drain becomes larger. The barrier for electron injection from the source to the channel is thus slightly decreased. Therefore, a conduction between the source and the drain occurs at a smaller gate overdrive leading to the reduction in the threshold voltage during the scaling.

In the on-current region, a drain current ($I_D$) is dominated by a drift transport of carriers [6]. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field in a small-geometry of NW-FETs. A potential barrier is controlled by both the gate-to-source voltage ($V_G$) and the drain-to-source voltage ($V_G$). If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electrons to flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage as it is shown in Fig. 5.20. Note that the channel current flow is under a condition $V_G > V_{Th}$ [6].

Table 5.5: The impact of threshold voltage on a channel length at different gate biases of $V_D$=1 V and 5 V.

| Channel length ($\mu$m) | Threshold voltage ($V_{Th}$) [V] at $V_G$= 1.0 V | Threshold voltage ($V_{Th}$) [V] at $V_G$= 5.0 V |
|---|---|---|
| 20 (2 NWs) | 6.7 | 8.3 |
| 10 (16 NWs) | 5.9 | 7.6 |
| 10 (2 NWs) | 5.3 | 5.65 |
| 2 (2 NWs) | 4.7 | 5.03 |

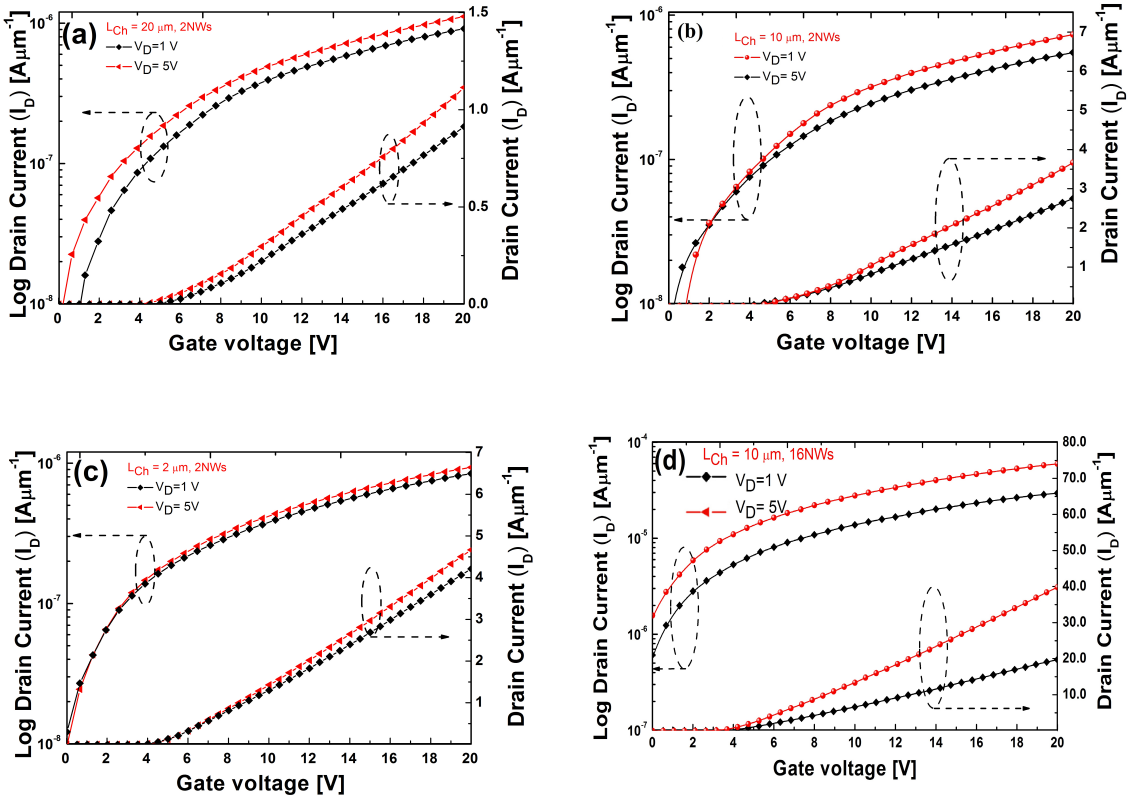


Figure 5.19: Transfer ($I_D$- $V_G$) characteristics under a drain bias of $V_D$= 1.0 V and 5.0 V for different channel lengths of (a) $L_{ch}$ =20 $\mu$m (2 NWs), (b ) $L_{ch}$ =10 $\mu$m (2NWs), (c) $L_{ch}$ = 2 $\mu$m (2 NWs), and (d) $L_{ch}$ = 10 $\mu$m (16 NWs).

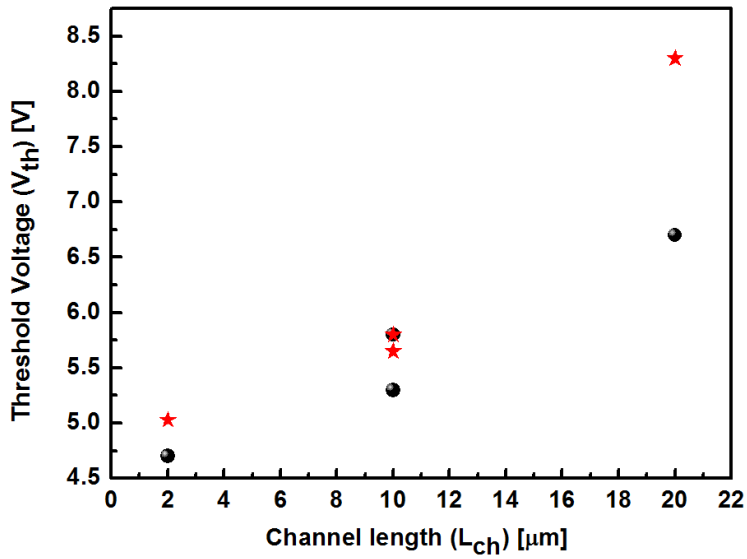


Figure 5.20: Variation of threshold voltage $V_{Th}$ as a function of the channel length. Figure shows the dependence between threshold voltage and channel length at different drain biases of 1.0 V (red stars) and 5.0 V (black circles).

## 5.7 Conclusion

ZnO TFTs have been fabricated by a top-down fabrication for different channel lengths (2 $\mu$m, 4 $\mu$m, 5 $\mu$m, and 10 $\mu$m). We have observed a decrease in the sub-threshold voltage with a channel length (10 $\mu$m to 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m) from (of 0.41, 0.57, 0.75, and 1.67 mV/dec, respectively). The contact resistance dependence on the channel length at two drain voltages (10.0 V and 15.0 V) was also studied. We have found that the contact resistance decrease with the increase of the gate voltage. As we increase the gate voltage, the contact resistance decreases. We have shown that the effective ($\mu_{\text{eff}}$) electron mobility decreases with scaling down of the source-to-drain distance. In addition, we have demonstrated that, channel ($\mu_{\text{ch}}$) electron mobility decreases with increase channel length, this is agree with the common expectations of ZnO TFTs [6].

The electron channel mobility summarised in Table 5.3. In addition, the Table shows a recent values have been calculated for ZnO TFTs by some previous reports. Our extracted values are between the range of the reported values in the previous reports [14].

The increase in the channel electron mobility during the channel scaling down the devices is indicative of a number of charge states along the thin film ZnO channel which will actively de-trap carriers thus increasing their intrinsic channel electron mobility. Despite the channel electron mobility increase in the scaled ZnO TFTs because of the increase of electron scattering with phonon and interface roughness due to increase in electric field along the channel. This enhanced channel mobility is a consequence of a higher kinetic energy of electrons ($E$) as $\exp^{(E/E_A)}$ where $E_A$ is the activation energy of channel mobility acquired from the increasing electric field. The increase in carriers will also act as scattering centres that increase the flow of carriers in the channel and increase the electron mobility due to remote Coulomb scattering [14].

Since the scattering will occur close to the conduction band edge, the increase in the applied bias (from 10.0 V to 15.0 V) with a larger kinetic energy will be able to move more effectively along the channel. Therefore, the electron channel mobility observed at 15.0 V is about three times larger than the mobility at 10.0 V for the 10 $\mu$m channel length device. However, the surface passivation can substantially mitigate this mobility increasing with scaling of the ZnO TFTs [2].

Furthermore, a top-down fabrication of ZnO NW-FETs ith different channel lengths (20 $\mu$m, 10 $\mu$m, and 2 $\mu$m) using the remote plasma ALD and the anisotropic reactive ion etching was also addressed. The optical characteristics measurements and SEM have been carried out. We have shown that the fabricated ZnO NWs have a horizontal alignment on the Al pad substrate. Moreover, we have measured the electrical characteristics using a probes technique. The $I_D$ –$V_D$ characteristics at gate biases of $V_G$ (2.0-20.0 V) have exhibited a typical transistor characteristics within $n$-type enhancement operation [6].

The ZnO NW-FETs have shown a linear regime at a low drain bias and a well saturated drain current regime at a high gate bias. However, when we have increased the gate bias up to 40.0 V, we have observed an early saturation in the transistor with a 2 $\mu$m channel length at a high gate bias of 5.0 V compared to the same channel length transistor at a low gate bias of 1.0 V. We have also studied the dependence between the channel length and the threshold voltage such that the threshold voltage decreases with the channel length decrease. In addition, we have observed that the maximum drain current scales as $1/L_{\mathrm{ch}}$ as expected. This agrees with a basic theory for MOSFETs [7].

# References


[1] *Southampton Nanotechnology Centre*. http://www.southampton-nanofab.com/. Accessed: 2018-02-12 (cit. on p. 91).

[2] S. M. Sultan, K. Sun, O. Clark, T. Masaud, Q. Fang, R. Gunn, J. Partridge, M. Allen, P. Ashburn, and H. Chong. "Electrical characteristics of top-down ZnO nanowire transistors using remote plasma ALD". In: *Electron Device Letters* 33.2 (2012), pp. 203–205 (cit. on pp. 91–94, 105, 110, 112–114, 117, 120).

[3] Z. Ye and M. Wong. "Characteristics of thin-film transistors fabricated on fluorinated zinc oxide". In: *Electron Device Letters* 33.4 (2012), pp. 549–551 (cit. on p. 94).

[4] M. D. Jacunski, M. S. Shur, and M. Hack. "Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFTs". In: *Transactions on Electron Devices* 43.9 (1996), pp. 1433–1440 (cit. on p. 95).

[5] Q. Zhang, J. Qi, Y. Yang, Y. Huang, X. Li, and Y. Zhang. "Electrical breakdown of ZnO nanowires in metal-semiconductor-metal structure". In: *Applied Physics Letters* 96.25 (2010), p. 253112 (cit. on pp. 95, 96).

[6] S. M. Sze and K. K. Ng. *Physics of semiconductor devices*. John Wiley and Sons, 2006 (cit. on pp. 97–99, 118, 120, 121).

[7] A. Ortiz-Conde, F. Sánchez, J. Liou, A. Cerdeira, M. Estrada, and Y. Yue. "A review of recent MOSFET threshold voltage extraction methods". In: *Microelectronics Reliability* 42.4 (2002), pp. 583–596 (cit. on pp. 99, 104, 106, 121).

[8] J. Gunho, M. Jongsun, K. Tae-Wook, H. Woong-Ki, J. Minseok, H. Hyunsang, and L. Takhee. "Effects of channel-length scaling on $In_2O_3$ nanowire field effect transistors studied by conducting atomic force microscopy". In: *Applied Physics Letters* 90 (2007), p. 173106 (cit. on p. 99).

[9] M. F. Al-Mistarihi, A. Rjoub, and N. R. Al-Taradeh. "Drain induced barrier lowering (DIBL) accurate model for nanoscale Si-MOSFET transistor". In: *25th International Conference on Microelectronics (ICM), 2013*. IEEE. 2013, pp. 1–4 (cit. on p. 99).

[10] H. Hsieh and C. Wu. "Scaling behavior of ZnO transparent thin-film transistors". In: *Applied Physics Letters* 89.4 (2006), p. 041109 (cit. on pp. 101, 103).

[11] J. Chern, P. Chang, R. F. Motta, and N. Godinho. "A new method to determine MOSFET channel length". In: *Electron Device Letters* 1.9 (1980), pp. 170–173 (cit. on pp. 101, 106).

[12] A. M. Lord, A. S. Walton, T. G. Maffeis, M. B. Ward, P. Davies, and S. P. Wilks. "ZnO Nanowires with Au Contacts Characterised in the as-Grown Real Device Configuration Using a Local Multi-Probe Method". In: *Nanotechnology* 25.42 (2014), p. 425706 (cit. on p. 101).

[13] G. K. Reeves and H. B. Harrison. "Obtaining the specific contact resistance from transmission line model measurements". In: *Transactions on Electron Devices* 3.5 (1972), pp. 111–113 (cit. on p. 104).

[14] Pimentel A. Pereira L. Gonalves-A. Lavareda G. Aguas H. Martins R. Fortunato E. "High field-effect mobility zinc oxide thin film transistors produced at room temperature". In: *Journal of Non-Crystalline Solids* 38.40 (2004), pp. 806–809 (cit. on pp. 105, 120).

[15] P. Carcia, R. McLean, and M. Reilly. "High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition". In: *Applied Physics Letters* 88.12 (2006), p. 123509 (cit. on p. 105).

[16] D. Kuzum, J. Park, T. Krishnamohan, H. P. Wong, and K. C. Saraswat. "The effect of donor acceptor nature of interface traps on Ge MOSFET characteristics". In: *Transactions on Electron Devices* 58.4 (2011), pp. 1015–1022 (cit. on p. 106).

[17] J. Sun, D. A. Mourey, D. Zhao, and T. N. Jackson. "ZnO thin film, device, and circuit fabrication using low-temperature PECVD processes". In: *Journal of Electronic Materials* 37.5 (2008), pp. 755–759 (cit. on p. 110).

[18] S. Ho, K. Chen, H. Chen, H. Lin, C. Cheng, and H. Lin. "Catalyst-Free Surface-Roughness-Assisted Growth of Large-Scale Vertically Aligned Zinc Oxide Nanowires by Thermal Evaporation". In: *Applied Physics Letters* 16.19 (2007), pp. 4083–4086 (cit. on p. 112).

[19] H. Woong-Ki, P. Jong-Bae, Y. Jongwon, K. Bong-Joong, S. Jung-Inn, L. Young-Boo, B. Tae-Sung, C. Sung-Jin, H. Yun-Suk, S. Byoungchul, A. S. Eric, L. Takhee, and E. W. Mark. "Tunable Electronic Transport Characteristics of Surface Architecture Controlled ZnO Nanowire Field Effect Transistors". In: *Nano Letters* 8.3 (2008), pp. 950–956 (cit. on p. 113).

[20] R. Timm, O. Persson, D. L. J. Engberg, A. Fian, J. L. Webb, J. Wallentin, A. Jónsson, M. T. Borgstrøm, L. Samuelson, and L. Mikkelsen. "Current-Voltage Characterization of Individual As-Grown Nanowires Using a Scanning Tunneling Microscope". In: *Nano Letter* 13.11 (2013), pp. 5182–5189 (cit. on p. 115).

[21] S. Chu, G. Wang, W. Zhou, Y. Lin, L. Chernyak, J. Zhao, J. Kong, L. Li, J. Ren, and J. Liu. "Electrically Pumped Waveguide Lasing from ZnO Nanowires". In: *Nature Nanotechnology* 33.6 (2011), pp. 506–510 (cit. on p. 117).

[22] Ü. Özgür, Y. I. Alivov, C. Liu, A. Teke, M. Reshchikov, S. Doğan, V. Avrutin, S. J. Cho, and H. Morkoc. "A comprehensive review of ZnO materials and devices". In: *Journal of Applied Physics* 98.4 (2005), p. 11 (cit. on p. 117).

# Chapter 6

# Conclusion and Future Work

## 6.1 Conclusion

In this thesis, we have presented a multi-scale simulation study of a nano-scale contact combining DFT calculations with solutions of 1D Poisson-Schrödinger (1DPS) equation aiming to understand a relation among a contact resistance and a band structure at the interface relevant to the future sub-10-nm technology. A multi-scale simulations study a nano-scale contact made of Ni metal interfacing an 11-nm thick InAs layer on a $p$-type doped $AlAs_{0.47}Sb_{0.53}$ buffer. A thermal reaction between Ni and InAs results in the formation of an 8.5 nm thick $Ni_3InAs$ layer leaving only a 2.5 nm thick of InAs acting as a channel material. The DFT calculations have revealed a band-gap narrowing in the InAs at metal-semiconductors interface inducing unexpected change of material properties of a semiconductor at the interface with a metal at nanoscale. The results give exceptionally good agreement with experimental observation of contact sheet resistance [1].

We have characterised ZnO TFTs which were fabricated by using a top-down fabrication method with different channel lengths 10 $\mu$m, 5 $\mu$m, 4 $\mu$m, and 2 $\mu$m) on thermally oxidized Si via remote plasma atomic layer deposition (PEALD). ZnO has been deposited over a $SiO_2$ pillar and anisotropically dry etched. The electrical characterisation has been carried out to study the impact of channel length ($L_{ch}$) scaling on contact resistance ($R_C$), and effective ($\mu_{\text{eff}}$) and channel ($\mu_{ch}$) electron mobility. We have also investigated the behaviour of breakdown voltage and sub-threshold voltage for each channel length and the impact of the scaling of channel length on threshold voltage. We have undergone through the electrical measurements of ZnO

TFTs using transmission line method (TLM) to obtain the access resistances, electron effective and electron channel mobility limiting current in the device. We have demonstrated that the contact resistance decreases with the increase of the gate voltage. We have shown that the effective ($\mu_{\text{eff}}$) electron mobility decreases with scaling down of the source-to-drain distance. However, the channel $\mu_{\text{ch}}$) electron mobility increases with the decrease in the channel length, this agree with the common expectations of ZnO TFTs [2, 3]. The increase in channel electron mobility when scaling down the channel length in ZnO TFTs is due to the increase in electric field along the channel. The electric field increases will lead to increase in kinetic energy of electrons. As a result, this increase in the electron kinetic energy reduces electron scattering with phonons, ionised impurities, and interface roughness.

We have also described the fabrication process for ZnO NWs field effect transistors (NWs-FETs) using a top-down fabrication. We have briefly showed that the top-down fabrication method starts with a thin film deposition by remote plasma enhanced atomic layer deposition (PEALD). The PEALD is followed by anisotropically reactive ion etch (RIE) to produce ZnO NWs with different channel lengths (20 $\mu$m, 10 $\mu$m, 2 $\mu$m). Optical and electrical characterisations were also carried out to study the scaling of channel length ($_{Lch}$) in the ZnO NW FETs transistors. The devices have demonstrated a linear regime at a low drain bias and a high saturation regime at a high drain bias with respect to all channel lengths. The $I_D$-$V_D$ characteristics at gate biases of $V_G$=2-20 V have exhibited a typical transistor characteristics within $n$-type enhancement operation. We have also studied the dependence between the channel lengths and the threshold voltage such that the threshold voltage decreases with the channel length decrease. We have observed that the maximum drain current scales as $1/L_{\text{ch}}$ as expected. This agrees with a basic theory for MOSFETs [3]. We have shown that the fabricated ZnO NWs have a horizontal alignment on the Al pad substrate. Moreover, we have measured the electrical characteristics using a probes technique.

## 6.2 Proposal for Future Work

The increasing development of semiconductor devices by many research groups created a various electronic and photonic applications such as computers (CPUs, memories), optical-storage media (lasers, CD, DVD), communication infrastructure (lasers

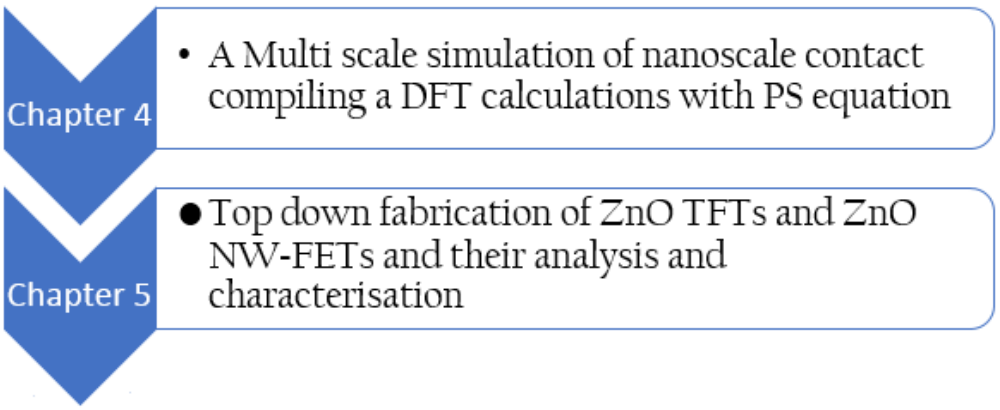


Figure 6.1: Illustration of the work demonstrated in this thesis.

and photo-detectors for optical-fibre technology, high frequency electronics for mobile communication), displays TFTs, LEDs), projection (laser diodes) and general lighting (LEDs). However, needs still remain to be addressed in electronic and photonic applications such as the contact made up of metal-semiconductor interfaces. The compatibility of metal and semiconductor components such as homogeneity structural and electrical characteristics of their interfaces and the durability of their contacts are crucial. It is well worth to study the optimal operation of contacts which is the key of realisation of novel devices and development of new device concepts including extension in the range of operation, lowering resistance of contacts, and enhancing mobility.

While the improvement and enhancement for these applications have been demonstrated, we believe that there are still needs to be addressed for further improvement. The following future recommendations can be listed as:

- Collaborate with Southampton University to study and develop a top-down fabrication method in order to grow ZnO via different substrate such as GaN, or InAs.

- Address and perform the ultra high vacuum of two-point probes measurement, that could be useful to measure the ZnO-TFTs and ZnO-NWs-FETs on Si substrates before putting down contacts which affect intrinsic properties of wires and thin-film on the substrate.

- Study the effect of annealing on nanowires and improve the surface contamination by using different enhancement methods such as ALD or plazma enhancement.

- Study and calculate the mobility of ZnO NW-FETs and compare to ZnO TFTs.
- Explore different gate dielectric materials such as $Al_2O_3$ in order to improve and enhance the mobility of ZnO TFTs and ZnO NW-FETs.
- Improve the 1DPS simulation tools by using different doping concentration to study the interface between a metal and a semiconductor.
- Develop PS simulation tools in 2D to calculate the density of state and extract a new contact resistance of different types of materials.

# References

[1] R. Oxland, S. Chang, X. Li, S. Wang, G. Radhakrishnan, W. Priyantha, M. J. H. Van Dal, C. H. Hsieh, G. Vellianitis, and G. Doornbos. "An ultralow resistance ultrashallow metallic source/drain contact scheme for III–V NMOS". In: *Electron Device Letters* 33.4 (2012), pp. 501–503 (cit. on p. 125).

[2] S. M. Sultan, K. Sun, O. Clark, T. B. Masaud, Q. Fang, R. Gunn, J. Partridge, M. Allen, P. Ashburn, and H. M. H. Chong. "Electrical characteristics of top-down ZnO nanowire transistors using remote plasma ALD". In: *Electron Device Letters* 33.2 (2012), pp. 203–205 (cit. on p. 126).

[3] H. Liu. *Intersubband Transitions in Quantum Wells: Physics and Device Applications*. 1999 (cit. on p. 126).